APPLICATION MANUAL

RV-2251-C3

Real-Time Clock / Calendar Module with I²C-bus interface

Date: January 2016 Revision N°: 1.0

A COMPANY OF THE SWATCH GROUP

Headquarters:
Micro Crystal AG
Mühlestrasse 14
CH-2540 Grenchen
Switzerland

Tel. +41 32 655 82 82
Fax +41 32 655 82 83
Internet www.microcrystal.com
Email sales@microcrystal.com

TABLE OF CONTENTS

RV-2251-C3

Real-Time Clock / Calendar Module with I²C-bus interface

1. OVERVIEW

- RTC Module with built-in “Tuning Fork” crystal oscillating at 32.768 kHz
- Counters for seconds, minutes, hours, date, weekday, month and year
- Programmable Offset register for frequency adjustment
- Automatic leap year calculation (2000 to 2099)
- Two Alarm Interrupt circuits:
  - Alarm_W for weekday, hour and minutes settings
  - Alarm_D for hour and minutes setting
- Periodic Time Update Interrupt function (2 Hz, 1 Hz, 1/60 Hz, 1/3600 Hz and monthly)
- Automatic Backup switchover function (V_{DD} monitoring)
- 3.0 V Regulated Output for ML rechargeable batteries (V_{REG})
- Monitoring function of backup power supply voltage (V_{BAT} monitoring)
- Built-in I²C-bus interface voltage detector with delayed access enable output (V_{IO} monitoring)
- Level shifter for I²C-bus interface and CLKOUT (V_{IO})
- Oscillator failure sensing function
- Internal Power-On Reset (POR)
- Power-On Reset Flag to prove that the power supply was started from 0V (V_{OUT})
- 32.768 kHz Clock Output
- I²C bus interface (up to 400 kHz)
- Wide Timekeeping voltage range: 0.9 V to 5.5 V
- Wide interface operating voltage: 1.9 to 5.5 V
- Low current consumption: 270 nA (V_{BAT} = 3.0 V)
  - Very low current consumption in ECO mode: 210 nA (V_{BAT} = 3.0 V)
- Operating temperature range: -40 to +85°C
- Small and compact C3 package size, RoHS-compliant and 100% lead-free: 3.7 x 2.5 x 0.9 mm

1.1. GENERAL DESCRIPTION

The RV-2251-C3 is a CMOS Real-Time Clock/Calendar Module with an automatic backup switchover circuit and a voltage detector. An Offset register allows compensating the frequency deviation of the 32.768 kHz clock. All addresses and data are transferred over an I²C-bus interface for communication with a host controller. The Address Pointer is incremented automatically after each written or read data byte. The low power consumption can even be lowered by selecting the ECO mode. 3.0 V ML rechargeable batteries can be directly connected to the RV-2251-C3.

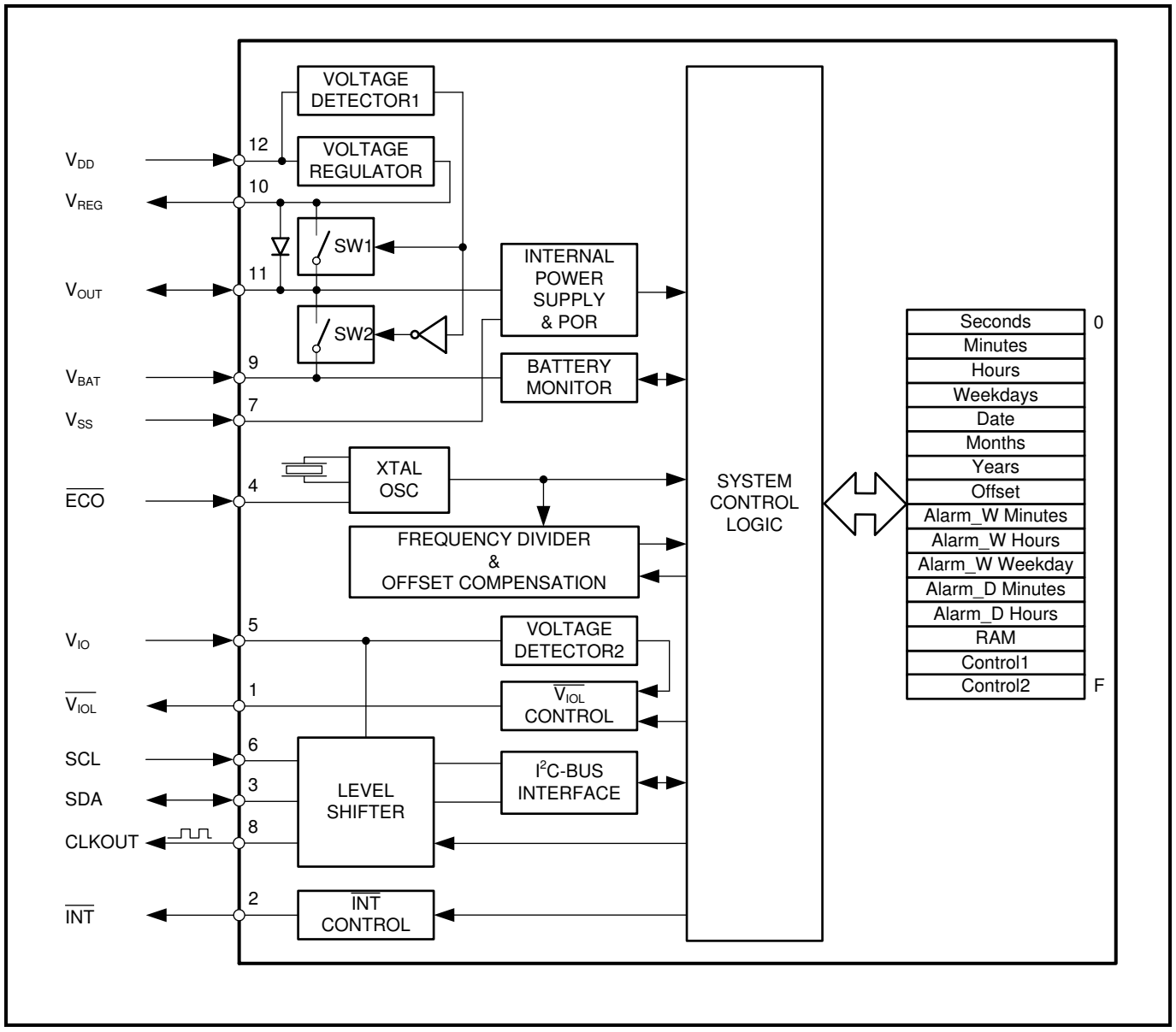
1.2. APPLICATIONS

The RV-2251-C3 RTC Module contains a backup switchover circuit to change automatically from main power source to back up power source according to needs.

This unique feature makes this product perfectly suitable for many applications:

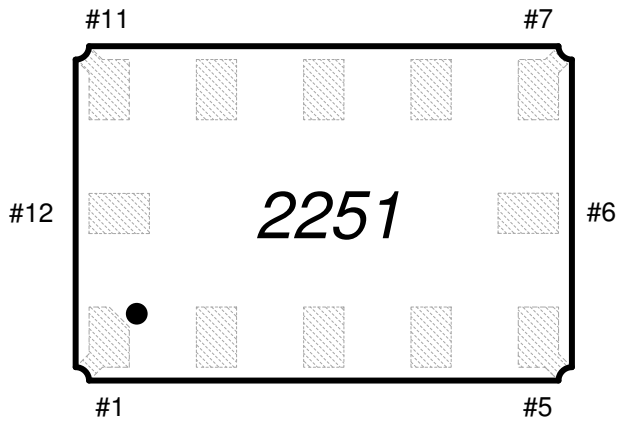
- Communication: IoT / Wearables / Wireless Sensors and Tags / Handsets
- Automotive: M2M / Navigation & Tracking Systems / Dashboard / Tachometers / Engine Controller Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter
- Outdoor: ATM & POS systems / Surveillance & Safety systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: DSLR / Security & Camera Systems / Door Lock & Access Control
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: DSC / Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

2. BLOCK DIAGRAM



2.1. PINOUT

C3 Package: (top view)



#1	$\overline{V_{IOL}}$
#2	$\overline{INT}$
#3	SDA
#4	$\overline{ECO}$
#5	V_{IO}
#6	SCL
#7	V_{SS}
#8	CLKOUT
#9	V_{BAT}
#10	V_{REG}
#11	V_{OUT}
#12	V_{DD}

2.2. PIN DESCRIPTION

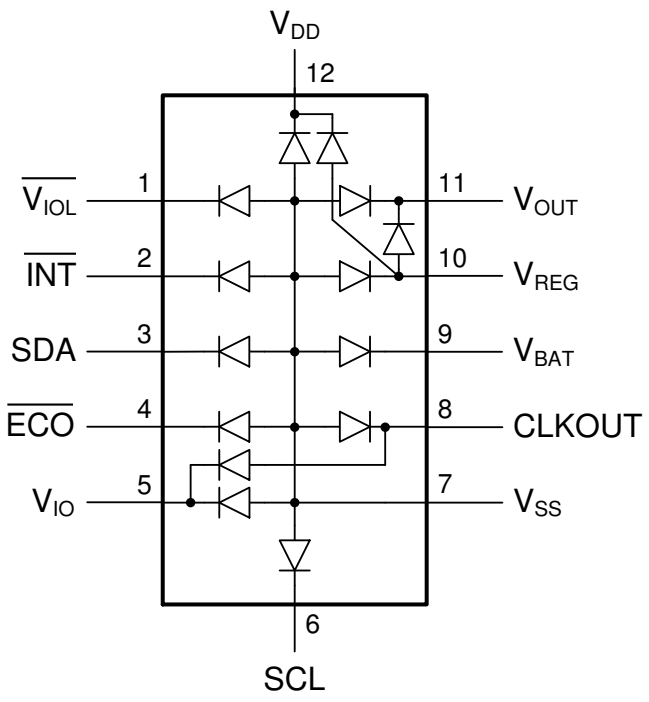
Symbol	Pin #	Description
$\overline{V_{IOL}}$	1	V_{IO} Peripheral Supply Monitoring Result Output; open-drain; active LOW; requires pull-up resistor. If V_{IO} voltage is equal or lower than V_{DET2F}, the $\overline{V_{IOL}}$ output level is LOW.
$\overline{INT}$	2	Interrupt Output; open-drain; active LOW; requires pull-up resistor. Used to output Alarm (Alarm_W and Alarm_D) and Periodic Time Update Interrupt signals.
SDA	3	I^2C Serial Data Input-Output; requires pull-up resistor. Is tolerant to 5.5 V regardless of power supply voltage.
$\overline{ECO}$	4	Input to select Oscillator mode. If $\overline{ECO}$ is HIGH, ECO mode is off. If $\overline{ECO}$ is tied to Ground, ECO mode is on. This pin must not be left floating or the RTC may consume higher current.
V_{IO}	5	Peripheral Supply Voltage Input (for I^2C interface and CLKOUT). Is tolerant to 5.5 V regardless of power supply voltage. If V_{IO} voltage is equal or lower than V_{DET2F}, the $\overline{V_{IOL}}$ output becomes LOW.
SCL	6	I^2C Serial Clock Input; requires pull-up resistor. Is tolerant to 5.5 V regardless of power supply voltage.
V_{SS}	7	Ground.
CLKOUT	8	32.768 kHz Clock Output; push-pull. Voltage of high level is equal to V_{IO}. Output always active.
V_{BAT}	9	Backup Power Supply Input. V_{BAT} can handle primary or secondary batteries or capacitors as backup sources. If V_{DD} level is equal or lower than V_{DET1F}, power is supplied from this pin. If V_{BAT} is not used, connect it to V_{OUT}. Do not connect V_{BAT} to V_{SS} (else V_{DD} is short circuited when $V_{DD} < V_{DET1F}$).
V_{REG}	10	Voltage regulator output. 3.0 V if $V_{DD} \geq 3.3$ V. Connect a 0.1 µF capacitor between V_{REG} and V_{SS}.
V_{OUT}	11	Internal Supply Voltage Output or Input. V_{OUT} is the switch-over output of V_{DD} and V_{BAT}. Directly input internal supply voltage over this pin is possible. Connect at least a 0.1 µF capacitor between V_{OUT} and V_{SS} when a secondary battery is connected to the pin V_{BAT}.
V_{DD}	12	Main Power Supply Input. If the voltage V_{DD} is equal or higher than V_{DET1R}, SW1 is closed, and SW2 is opened. As a result, power is supplied by V_{DD} pin. If the voltage V_{DD} is equal or lower than V_{DET1F}, SW1 is open, and SW2 turns on. As a result, power is supplied from V_{BAT} pin.

2.3. FUNCTIONAL DESCRIPTION

The RV-2251-C3 is a low power CMOS based Real-Time Clock Module with embedded 32.768 kHz Crystal.
The RTC module is specially designed for versatile backup solutions. The multi-functionality of the RV-2251-C3 is reached with the Automatic Backup switchover function, a separate Peripheral Supply Voltage Input with level shifter, a monitoring function of the backup power supply voltage and a 3.0 V Regulated Output for charging ML rechargeable batteries (e.g. Renata LMR 2016) or capacitors.
Additionally, there is an Offset Register customer use for aging correction.

The RTC Module provides standard Clock & Calendar function including seconds, minutes, hours (12 or 24 h), weekday, date, months, years (with automatic leap year calculation) and an interrupt function with two programmable Alarm settings and a Periodic Time Update Interrupt function. Beside the standard RTC functions it includes 1 Byte of User RAM and offers an I^2C-bus (2-wire interface).
The registers are accessed by selecting a register address with the Address Pointer and the Transmission Format and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the Address Pointer automatically incrementing after each byte.

2.4. DEVICE PROTECTION DIAGRAM



3. REGISTER ORGANIZATION

Registers are accessed by selecting a register address including the 4-bit Address Pointer and the 4-bit Transmission Format and then performing read or write operations (see REGISTER ADDRESS). Multiple reads or writes may be executed in a single access, with the Address Pointer automatically incrementing after each byte.
16 registers (Address Pointer 0h – Fh) are available. The time registers are encoded in the Binary Coded Decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary format. When one of the RTC registers is written or read, the contents of all time counters are frozen for up to 0.5 second. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

3.1. REGISTER OVERVIEW

After reset, all registers are set according to Table in section REGISTER RESET VALUES SUMMARY.

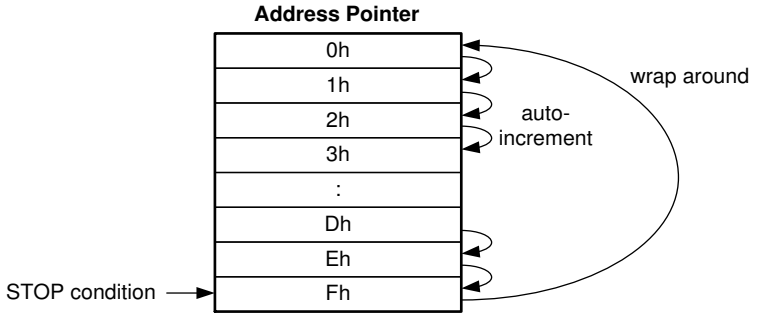
Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	Seconds	○	40	20	10	8	4	2	1
1h	Minutes	○	40	20	10	8	4	2	1
2h	Hours	○	○	AMPM	10	8	4	2	1
				20	10	8	4	2	1
3h	Weekday	○	○	○	○	○	4	2	1
4h	Date	○	○	20	10	8	4	2	1
5h	Months	○	○	○	10	8	4	2	1
6h	Years	80	40	20	10	8	4	2	1
7h	Offset	MODE	OFFSET						
8h	Alarm_W Minutes	○	40	20	10	8	4	2	1
9h	Alarm_W Hours	○	○	AMPM	10	8	4	2	1
				20	10	8	4	2	1
Ah	Alarm_W Weekdays	○	6	5	4	3	2	1	0
Bh	Alarm_D Minutes	○	40	20	10	8	4	2	1
Ch	Alarm_D Hours	○	○	AMPM	10	8	4	2	1
				20	10	8	4	2	1
Dh	RAM	RAM data							
Eh	Control1	AE_W	AE_D	12_24	GP0	TEST	USEL		
Fh	Control2	GP1	BLF	OF	PON	GP2	UF	WF	DF

○ Bit not implemented. Will return a 0 when read.

3.1.1. AUTO-INCREMENTING AND STOP CONDITION

When address is automatically incremented, wrap around occurs from the Address Pointer value Fh to value 0h (see figure below). Note that the Address Pointer is set to Fh when sending an I^2C STOP condition (see START AND STOP CONDITIONS).

Auto-incrementing of the Address Pointer, and I^2C STOP condition:



3.2. TIME AND DATE REGISTERS

0h - Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	Seconds	○	40	20	10	8	4	2	1
	Reset	0	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7	○	0	Unused
6:0	Seconds	00 to 59	Holds the count of seconds, coded in BCD format.

1h - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1h	Minutes	○	40	20	10	8	4	2	1
	Reset	0	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7	○	0	Unused
6:0	Minutes	00 to 59	Holds the count of minutes, coded in BCD format.

2h - Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. If the 12_24 bit is clear (see CONTROL REGISTERS, Eh - Control1) the values will be from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. If the 12_24 bit is set, the hour values will range from 0 to 23.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2h	Hours (12 hour mode)	○	○	AMPM	10	8	4	2	1
	Hours (24 hour mode)			20	10	8	4	2	1
	Reset	0	0	X	X	X	X	X	X

Hours (12 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5	AMPM	0	AM hours.
		1	PM hours.
4:0	Hours (12 hour mode)	1 to 12	Holds the count of hours, coded in BCD format.

Hours (24 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5:0	Hours (24 hour mode)	0 to 23	Holds the count of hours, coded in BCD format.

3h - Weekday

This register holds the current day of the week. Each value represents one weekday that is assigned by the user. Values will range from 0 to 6.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3h	Weekday	○	○	○	○	○	4	2	1
	Reset	0	0	0	0	0	X	X	X

Bit	Symbol	Value	Description
7:3	○	0	Unused
2:0	Weekday	0 to 6	Holds the weekday counter value.

Weekday	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Weekday 1	0	0	0	0	0	0	0	0
Weekday 2						0	0	1
Weekday 3						0	1	0
Weekday 4						0	1	1
Weekday 5						1	0	0
Weekday 6						1	0	1
Weekday 7						1	1	0

4h – Date

This register holds the current date of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4h	Date	○	○	20	10	8	4	2	1
	Reset	0	0	X	X	X	X	X	X

Bit	Symbol	Value	Description
7:6	○	0	Unused
5:0	Date	01 to 31	Holds the current date of the month, coded in BCD format.

5h - Months

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5h	Months	○	○	○	10	8	4	2	1
	Reset	0	0	0	X	X	X	X	X

Bit	Symbol	Value	Description
7:5	○	0	Unused
4:0	Months	01 to 12	Holds the current month, coded in BCD format.

Months	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	0	0	0	1
February				0	0	0	1	0
March				0	0	0	1	1
April				0	0	1	0	0
May				0	0	1	0	1
June				0	0	1	1	0
July				0	0	1	1	1
August				0	1	0	0	0
September				0	1	0	0	1
October				1	0	0	0	0
November				1	0	0	0	1
December				1	0	0	1	0

6h - Years

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99. Leap years are correctly handled from 2000 to 2099.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6h	Years	80	40	20	10	8	4	2	1
	Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7:0	Years	00 to 99	Holds the current year, coded in BCD format.

3.3. OFFSET REGISTER

7h – Offset Register

This register holds the OFFSET value to digitally compensate the initial frequency deviation of the 32.768 kHz oscillator or for aging adjustment (see FREQUENCY OFFSET COMPENSATION).

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7h	Offset	MODE	OFFSET						
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	MODE		Offset Mode
		0	Normal Mode: Offset is compensated every 20 seconds (at 00, 20 and 40).
		1	Slow Mode: Offset is compensated every minute (at seconds = 00).
6:0	OFFSET	-62 to +62	Defines compensation pulses in steps. For MODE = 0, each pulse introduces a deviation of 3.052 ppm, the maximum range is ±189 ppm. For MODE = 1, each pulse introduces a deviation of 1.017 ppm, the maximum range is ±63 ppm. The values of 3.052 ppm and 1.017 ppm are based on a nominal 32.768 kHz clock (see FREQUENCY OFFSET COMPENSATION).

OFFSET	OFFSET compensation value in decimal	Converting (mathematical operation)	Compensation pulses in steps	CLKOUT frequency deviation in ppm(2)	
				Normal Mode MODE = 0	Slow Mode MODE = 1
0111111	+63	-1	+62	+189.209	+63.070
0111110	+62	-1	+61	+186.157	+62.052
:	:	:	:	:	:
0000011	+3	-1	+2	+6.104	+2.035
0000010	+2	-1	+1	+3.052	+1.017
0000001 (1)	+1	×0	0	0	0
0000000 (1)	0				
1111111	+127	Two's complement	-1	-3.052	-1.017
1111110	+126	Two's complement	-2	-6.104	-2.035
:	:	:	:	:	:
1000011	+67	Two's complement	-61	-186.157	-62.052
1000010	+66	Two's complement	-62	-189.209	-63.070
1000001 (1)	+65	×0	0	0	0
1000000 (1)	+64				

(1) The OFFSET values X00000X mean no correction steps are done (X representing 0 or 1) and the offset circuit is disabled. With this converting method a symmetrical structure of ±62 correction steps can be guaranteed.

(2) For MODE = 0, each compensation pulse corresponds to 1/(32768×10) = 3.052 ppm. For MODE = 1 it is 1/(32768×30) = 1.017 ppm. The frequency deviation measured at CLKOUT pin can be compensated by computing the compensation value OFFSET and writing it into the Offset register (see OFFSET COMPENSATION CALCULATION WORKFLOW).

3.4. ALARM_W REGISTERS

8h – Alarm_W Minutes

This register holds the alarm value for minutes for Alarm_W, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8h	Alarm_W Minutes	○	40	20	10	8	4	2	1
	Reset	0	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7	○	0	Unused
6:0	Alarm_W Minutes	00 to 59	Holds the alarm value for minutes for Alarm_W, coded in BCD format.

9h – Alarm_W Hours

This register holds the alarm value for hours for Alarm_W, in two binary coded decimal (BCD) digits. If the 12_24 bit is clear (see CONTROL REGISTERS, Eh - Control1) the values will be from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. If the 12_24 bit is set, the hour values will range from 0 to 23.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9h	Alarm_W Hours (12 hour mode)	○	○	AMPM	10	8	4	2	1
	Alarm_W Hours (24 hour mode)			20	10	8	4	2	1
	Reset	0	0	X	X	X	X	X	X

Alarm_W Hours (12 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5	AMPM	0	AM hours.
		1	PM hours.
4:0	Alarm_W Hours (12 hour mode)	1 to 12	Holds the alarm value for hours for Alarm_W, coded in BCD format.

Alarm_W Hours (24 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5:0	Alarm_W Hours (24 hour mode)	0 to 23	Holds the alarm value for hours for Alarm_W, coded in BCD format.

Ah – Alarm_W Weekdays

This register holds the alarm value for the weekdays for Alarm_W (weekdays assigned by the user). Multiple days can be selected. Values will range from 0000001 to 1111111.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ah	Alarm_W Weekdays	○	6	5	4	3	2	1	0
	Reset	0	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7	○	0	Unused
6:0	Alarm_W Weekdays	0000001 to 1111111	Holds the weekday alarm value for Alarm_W. Multiple days can be selected.

Alarm_W Weekdays	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Alarm_W Weekday 1	0	0	0	0	0	0	0	1
Alarm_W Weekday 2		0	0	0	0	0	1	0
Alarm_W Weekday 3		0	0	0	0	1	0	0
Alarm_W Weekday 4		0	0	0	1	0	0	0
Alarm_W Weekday 5		0	0	1	0	0	0	0
Alarm_W Weekday 6		0	1	0	0	0	0	0
Alarm_W Weekday 7		1	0	0	0	0	0	0

3.5. ALARM_D REGISTERS

Bh – Alarm_D Minutes

This register holds the alarm value for minutes for Alarm_D, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bh	Alarm_D Minutes	○	40	20	10	8	4	2	1
	Reset	0	X	X	X	X	X	X	X

Bit	Symbol	Value	Description
7	○	0	Unused
6:0	Alarm_D Minutes	00 to 59	Holds the alarm value for minutes for Alarm_D, coded in BCD format.

Ch – Alarm_D Hours

This register holds the alarm value for hours for Alarm_D, in two binary coded decimal (BCD) digits. If the 12_24 bit is clear (see CONTROL REGISTERS, Eh - Control1) the values will be from 1 to 12 and the AMPM bit will be 0 for AM hours and 1 for PM hours. If the 12_24 bit is set, the hour values will range from 0 to 23.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ch	Alarm_D Hours (12 hour mode)	○	○	AMPM	10	8	4	2	1
	Alarm_D Hours (24 hour mode)			20	10	8	4	2	1
	Reset	0	0	X	X	X	X	X	X

Alarm_D Hours (12 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5	AMPM	0	AM hours.
		1	PM hours.
4:0	Alarm_D Hours (12 hour mode)	1 to 12	Holds the alarm value for hours for Alarm_D, coded in BCD format.

Alarm_D Hours (24 hour mode)

Bit	Symbol	Value	Description
7:6	○	0	Unused
5:0	Alarm_D Hours (24 hour mode)	0 to 23	Holds the alarm value for hours for Alarm_D, coded in BCD format.

3.6. RAM REGISTER

Dh - RAM

Free RAM byte, which can be used for any purpose, for example, status byte of the system.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dh	RAM	RAM data							
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	RAM	00h to FFh	User RAM

3.7. CONTROL REGISTERS

Eh - Control1

Control and status register 1.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Eh	Control1	AE_W	AE_D	12_24	GP0	TEST	USEL		
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_W	Alarm_W Interrupt Enable (see ALARM FUNCTION and INTERRUPT SUMMARY)	
		0	Disabled
		1	Enabled
6	AE_D	Alarm_D Interrupt Enable (see ALARM FUNCTION and INTERRUPT SUMMARY)	
		0	Disabled
		1	Enabled
5	12_24	12 or 24 hour mode (see TIME AND DATE REGISTERS, ALARM_W REGISTERS and ALARM_D REGISTERS)	
		0	12 hour mode is selected (1 to 12).
		1	24 hour mode is selected (0 to 23).
4	GP0	0 or 1	Register bit for general purpose use.
3	TEST	0	Normal mode.
		1	Test mode. Do not use.
2:0	USEL	000 to 111	Periodic Time Update Interrupt selection (see PERIODIC TIME UPDATE INTERRUPT FUNCTION and INTERRUPT SUMMARY)

USEL	USEL-Mode	$\overline{INT}$ Frequency
000	-	OFF ($\overline{INT}$ = HIGH) – Default value
001	-	Always ON ($\overline{INT}$ = LOW) (1)
010	Pulse	2 Hz (2) (3)
011	Pulse	1 Hz (2) (3)
100	Level	Every second (3)
101	Level	Every minute
110	Level	Every hour
111	Level	Every month

(1) When USEL = 001b the flag UF cannot be reset to 0.

(2) Duty cycle = 50%

(3) In Pulse Mode the 2 Hz and 1 Hz clock pulses and in Level Mode the 1 Hz signal can be affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

Fh – Control2

Control and status register 2.

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Fh	Control2	GP1	BLF	OF	PON	GP2	UF	WF	DF
	Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Value	Description
7	GP1	0 or 1	Register bit for general purpose use.
6	BLF		Battery Low Flag (see VBAT MONITORING CIRCUIT)
		0	Backup Power Supply voltage V_{BAT} is above the threshold value V_{BLF}.
		1	Backup Power Supply voltage V_{BAT} dropped below the threshold value V_{BLF}. It can be cleared by writing a 0 to the bit. This bit is also set on a power on reset (POR) and can be cleared by writing a 0 to the bit.
5	OF		Oscillator Failure Flag (see OSCILLATOR FAILURE DETECTION
		0	No oscillator failure has occurred.
		1	Oscillator Failure. This bit is set if an oscillator failure occurs. It can be cleared by writing a 0 to the bit. This bit is also set on a power on reset (POR) and can be cleared by writing a 0 to the bit.
4	PON		Power-On reset Flag (see POWER-ON RESET)
		0	No Power-On reset state detected.
		1	V_{OUT} Power-On reset state (POR) detected. All registers are initialized to their reset values. It can be cleared by writing a 0 to the bit.
3	GP2	0 or 1	Register bit for general purpose use.
2	UF		Periodic Time Update Interrupt Flag (see PERIODIC TIME UPDATE INTERRUPT FUNCTION and INTERRUPT SUMMARY)
		0	Periodic Time Update Interrupt output $\overline{INT}$ is inactive (HIGH).
		1	Periodic Time Update Interrupt output $\overline{INT}$ is active (LOW). It can be cleared by writing a 0 to the bit only in the Level Mode (see LEVEL MODE), which deactivates the $\overline{INT}$ pin (goes HIGH) until it is activated (tied LOW) again in the next interrupt cycle.
1	WF		Alarm_W Flag (see ALARM FUNCTION and INTERRUPT SUMMARY)
		0	No match detected.
		1	Indicating a match between current time and preset alarm time. The WF bit is only valid when AE_W = 1 and approximately 15 µs after the Alarm_W registers match their respective counters. It can be cleared by writing a 0 to the bit.
0	DF		Alarm_D Flag (see ALARM FUNCTION and INTERRUPT SUMMARY)
		0	No match detected.
		1	Indicating a match between current time and preset alarm time. The DF bit is only valid when AE_D = 1 and approximately 15 µs after the Alarm_D registers match their respective counters. It can be cleared by writing a 0 to the bit.

3.8. REGISTER RESET VALUES SUMMARY

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	Seconds	0	X	X	X	X	X	X	X
1h	Minutes	0	X	X	X	X	X	X	X
2h	Hours	0	0	X	X	X	X	X	X
3h	Weekday	0	0	0	0	0	X	X	X
4h	Date	0	0	X	X	X	X	X	X
5h	Months	0	0	0	X	X	X	X	X
6h	Years	X	X	X	X	X	X	X	X
7h	Offset	0	0	0	0	0	0	0	0
8h	Alarm_W Minutes	0	X	X	X	X	X	X	X
9h	Alarm_W Hours	0	0	X	X	X	X	X	X
Ah	Alarm_W Weekdays	0	X	X	X	X	X	X	X
Bh	Alarm_D Minutes	0	X	X	X	X	X	X	X
Ch	Alarm_D Hours	0	0	X	X	X	X	X	X
Dh	RAM	0	0	0	0	0	0	0	0
Eh	Control1	0	0	0	0	0	0	0	0
Fh	Control2	0	1	1	1	0	0	0	0
X means undefined.									

RV-2251-C3 after power-on reset:

Time (hh:mm:ss)	=	XX:XX:XX
Date (YY-MM-DD)	=	XX-XX-XX
Weekday	=	X
Hour mode	=	12 hour mode (AM/PM)
Offset	=	Offset register is set to 0
Periodic Interrupt	=	disabled
Alarms	=	disabled
Battery Low Flag	=	1 (can be cleared by writing a 0 to the bit)
Oscillator Failure Flag	=	1 (can be cleared by writing a 0 to the bit)
Power-On reset Flag	=	1 (can be cleared by writing a 0 to the bit)

4. DETAILED FUNCTIONAL DESCRIPTION

4.1. AUTOMATIC BACKUP SWITCHOVER FUNCTION

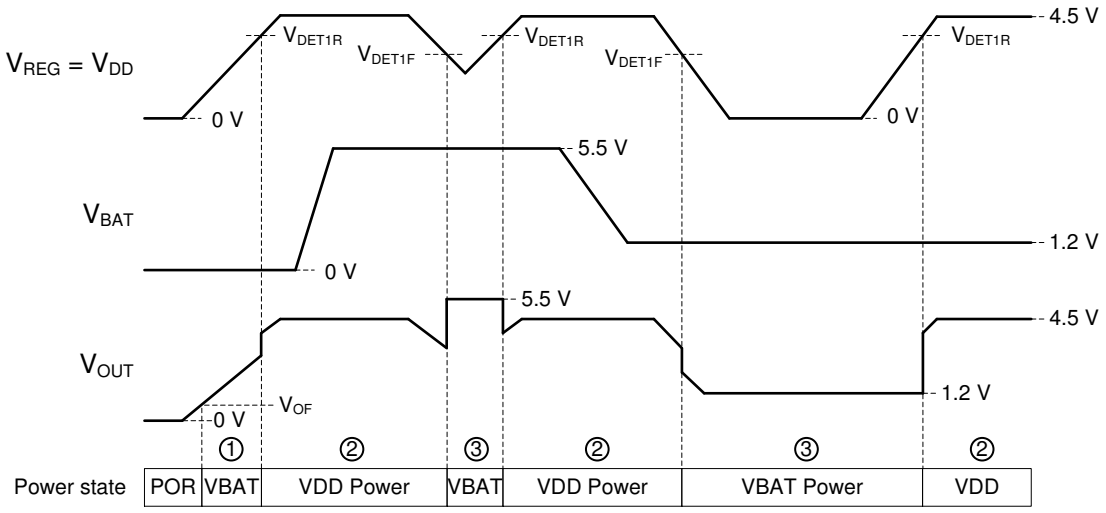
The RV-2251-C3 has two power supply inputs, V_{DD} and V_{BAT}, to supply the RTC circuit with the XTAL. By monitoring the input voltage V_{DD} with the internal Voltage Detector 1, it is selected which of the two power supplies is used for the internal power source V_{OUT}. When V_{DD} voltage is lower than V_{DET1}, V_{BAT} supplies the power to V_{OUT}, and when higher than V_{DET1}, V_{DD} supplies the power to V_{OUT} (see also VDD MONITORING CIRCUIT).
The following table shows the power state of the IC as a function of the V_{DD} supply voltage.

Automatic Backup Switchover:

Condition	Power state	Description
$V_{DD} > V_{DET1}$	VDD Power	V_{OUT} connected to V_{DD}. SW1 is closed, and SW2 is open.
$V_{DD} \leq V_{DET1}$	VBAT Power	V_{OUT} connected to V_{BAT}. SW1 is open, and SW2 is closed.

As a backup source not only a primary battery such as CR2025, LR44, or a secondary battery such as ML614, but also an electric double layer capacitor or an aluminum electrolytic capacitor can be applied. Since the switchover point is judged with the voltage level of the main power supply V_{DD}, it allows the RV-2251-C3 to minimize the current drawn from the V_{BAT} supply by switching to V_{BAT} only at the point where V_{DD} is no longer able to power the device. See following timing chart for V_{DD}, V_{BAT}, and V_{OUT}.

Backup switchover timing example: $V_{REG} = V_{DD} = 4.5$ V



① When V_{BAT} is 0 V and V_{DD} is rising from 0 V, V_{OUT} follows about the half of V_{DD} voltage level (over SW1 protective diode). Once V_{OUT} has reached V_{OF}, RV-2251-C3 switches to V_{BAT} (SW1 = OFF, SW2 = ON). However, because $V_{OUT} > V_{BAT}$, V_{OUT} is supplied by $V_{REG} = V_{DD}$ over SW1 protective diode. After V_{DD} rising over V_{DET1R}, V_{OUT} follows V_{DD} voltage level.

② When V_{DD} is higher than V_{DET1R}, V_{OUT} is connected to V_{DD} (SW1 = ON, SW2 = OFF).

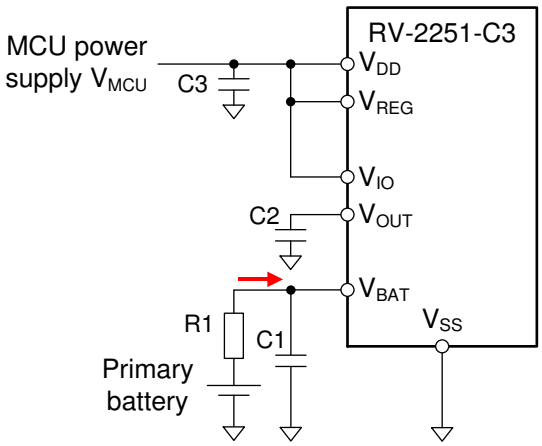
③ After V_{DD} falling beyond V_{DET1F}, V_{OUT} is connected to V_{BAT} (SW1 = OFF, SW2 = ON).

Note: In this circuit where backup is done with primary battery and V_{BAT} is not hard-wired to V_{OUT}, the switchover to V_{BAT} (SW2 closed) can only occur after a previous startup of V_{DD}. A voltage V_{DD} of 1.0 V is sufficient, and it can be turned off again after start-up time t_{START}. With this circuit, it is not possible to power on from V_{BAT} only (see PRIMARY BATTERY).

4.1.1.PRIMARY BATTERY

Backup with primary battery: Conditions V_{MCU}, V_{BAT}

With primary battery e.g. CR2025 or LR44 (V_{BAT} = 3.0 V).

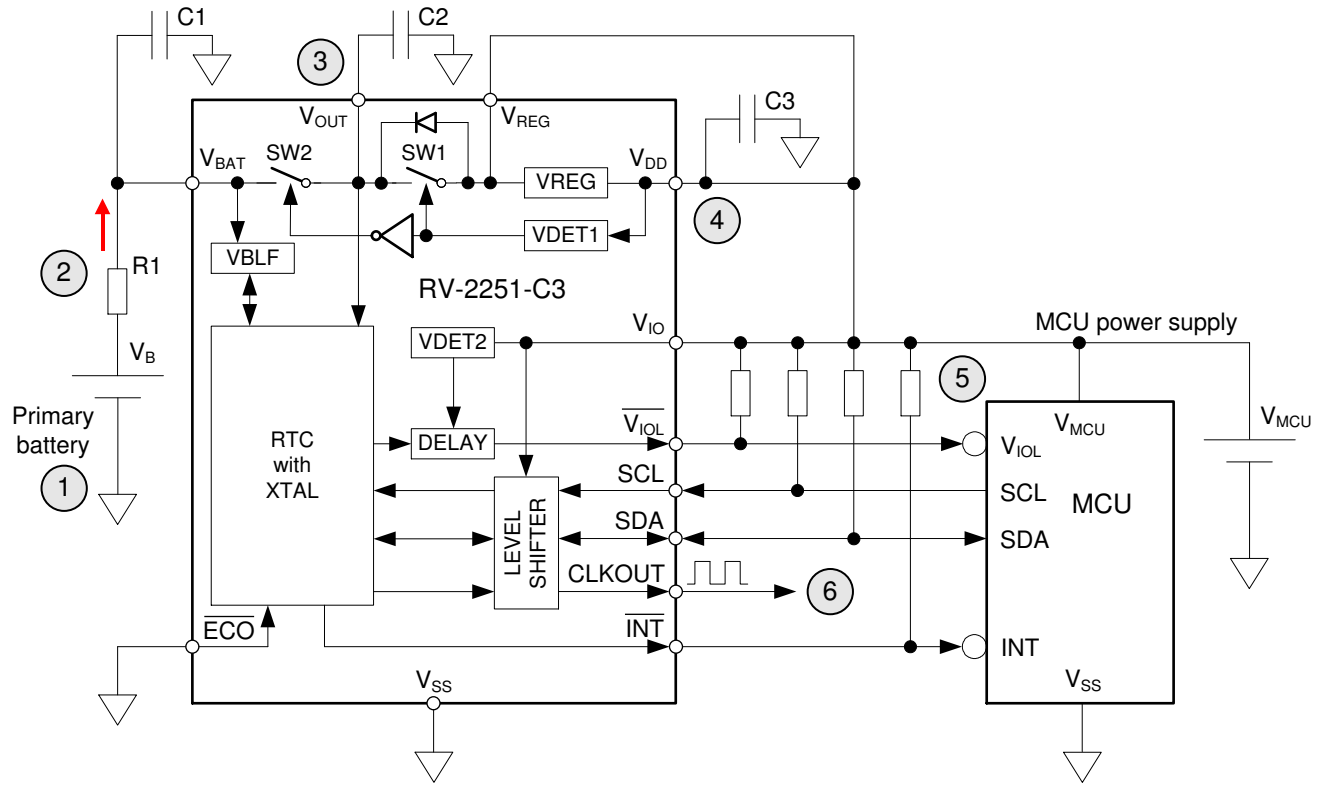


Power state and interface access:

- V_{OUT} powered from 0 V to 0.7 V with V_{MCU} from 0 V to 1.0 V (with V_{BAT} NOT POSSIBLE!)
  - POR state
  - Interface access disabled
- V_{MCU} between 1.0 V and V_{DET2R} (typ. 1.77 V):
  - VBAT Power state
  - Interface access disabled
- V_{MCU} between V_{DET2R} (typ. 1.77 V) and V_{DET1R} (typ. 2.78 V) AND V_{BAT} between 1.0 V and 5.5 V:
  - VBAT Power state
  - Interface access enabled
- V_{MCU} between V_{DET1R} (typ. 2.78 V) and 5.5 V
  - VDD Power state
  - Interface access enabled

Note: In this circuit where backup is done with primary battery and V_{BAT} is not hard-wired to V_{OUT}, the switchover to V_{BAT} (SW2 closed) can only occur after a previous startup of V_{DD}. A voltage V_{DD} of 1.0 V is sufficient, and it can be turned off again after the start-up time t_{START}. With this circuit, it is not possible to power on from V_{BAT} only.

Backup with primary battery: All components



1 Primary battery e.g. CR2025 or LR44 (V_{BAT} = 3.0 V).

2 When using a primary battery, a series resistor R1 is used to limit battery current and to prevent damage in case of soldering issues causing short between supply pins.

3 A 100 nF decoupling capacitor (C1, C2 and C3) is recommended close to the device for every power supply pin (here V_{REG}, V_{DD} and V_{IO} together).

4 Main RTC Power Supply. If the voltage is equal or lower than V_{DET1F}, SW1 is open, and SW2 turns on. As a result, power is supplied from V_{BAT} pin. When V_{DD} is equal or higher than V_{DET1R}, SW1 is closed, and SW2 is opened.

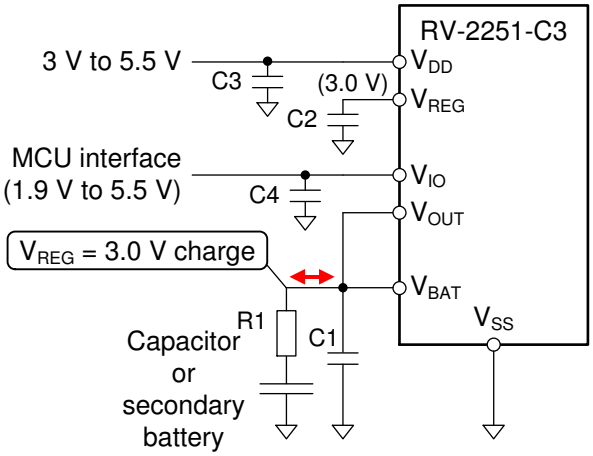
5 Interface lines SCL, SDA and the outputs $\overline{V_{IOL}}$ and $\overline{INT}$ are open drain and require pull-up resistors to V_{IO}.

6 32.768 kHz Clock Output; push-pull. Voltage of high level is equal to V_{IO}. Output always active.

4.1.2.CAPACITOR OR SECONDARY BATTERY 3.0 V CHARGE

Backup with capacitor or secondary battery, 3.0 V charge: Conditions V_{DD}, V_{BAT}, V_{IO}

E.g. with secondary battery ML614 Manganese Rechargeable Lithium Battery (ML series).
Charging voltage is V_{REG} = 3.0 V.



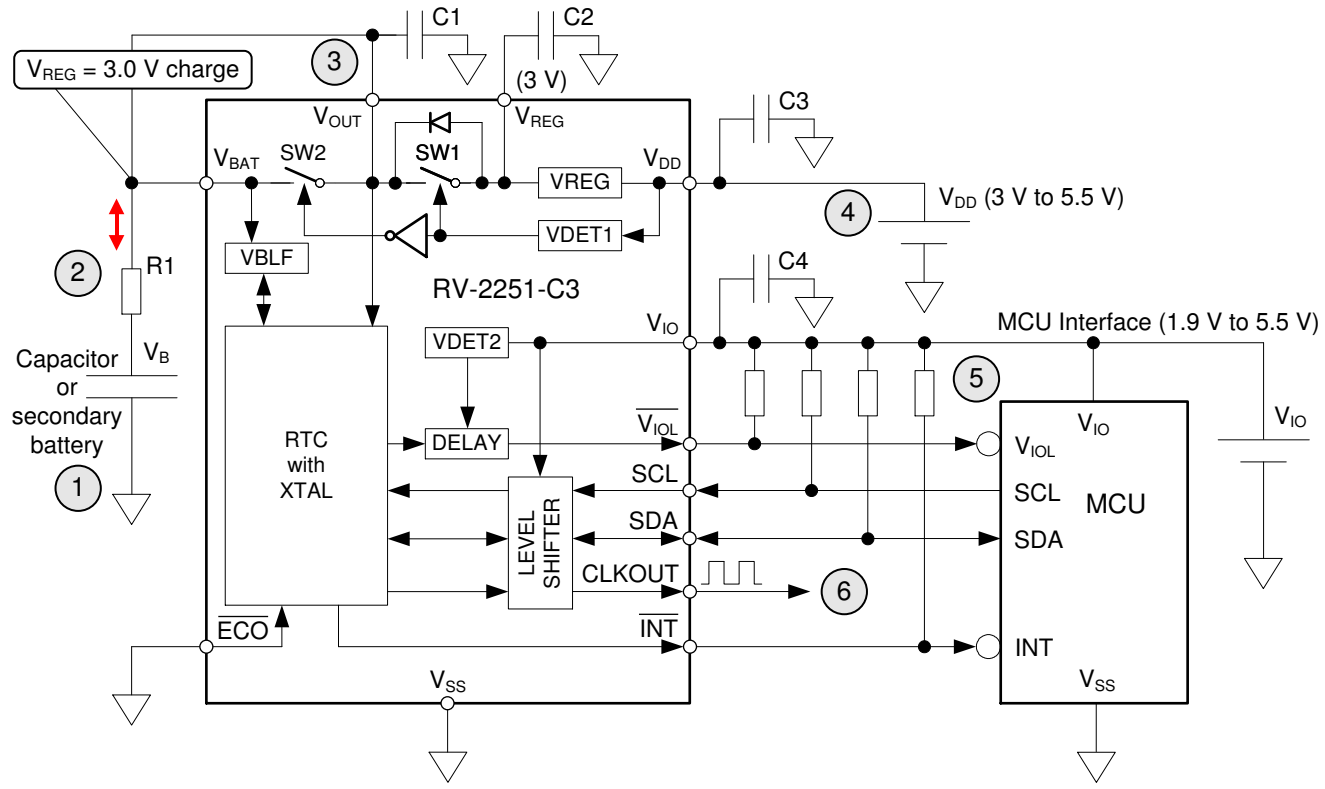
Power state:

- V_{OUT} powered from 0 V to 0.7 V with V_{DD} from 0 V to 1.0 V OR with V_{BAT} from 0 V to 0.7 V
  - POR state
- V_{DD} between 1.0 V and V_{DET1R} (typ. 2.78 V):
  - VBAT Power state
  - Discharging secondary battery down to V_{DD}
- V_{DD} between V_{DET1R} (typ. 2.78 V) and 3.0 V:
  - VDD Power state
  - Charging secondary battery to V_{DD}
- V_{DD} between 3.0 V and 5.5 V
  - VDD Power state
  - Charging secondary battery with regulated voltage V_{REG} = 3.0 V

MCU interface access:

- V_{IO} between 0 V and V_{DET2R} (typ. 1.77 V):
  - Interface access disabled
- V_{IO} between V_{DET2R} (typ. 1.77 V) and 5.5 V AND V_{OUT} between 1.0 V and 5.5 V (powered from V_{DD} or V_{BAT}):
  - Interface access enabled

Backup with capacitor or secondary battery, 3.0 V charge: All components



1 Supercapacitor (e.g. 1 farad) or secondary battery. e.g. ML614 Manganese Rechargeable Lithium Battery (ML series). Charging voltage is V_{REG} = 3.0 V.

2 When using a supercapacitor, a series resistor R1 is used to limit the inrush current into the supercapacitor at power-on. E.g. to comply with the maximum output current of the RV-2251-C3 (I_{Omax} = 10 mA).
To limit the current to comply with the specification of the backup device.
And to fulfill the condition R1 > R_{MCU} * (V_B – (V_{DET1F})) / V_{DET1F}) that after switch off the MCU the voltage V_{DD} is falling below V_{DET1F} for shore and RV-2251-C3 can switch SW1 OFF.

3 A 100 nF decoupling capacitor (C1, C2, C3 and C4) is recommended close to the device for every power supply pin (V_{BAT} and V_{OUT} together).

4 Main RTC Power Supply. If the voltage is equal or lower than V_{DET1F}, SW1 is open, and SW2 turns on. As a result, power is supplied from V_{BAT} pin. When V_{DD} is equal or higher than V_{DET1R}, SW1 is closed, and SW2 is opened.

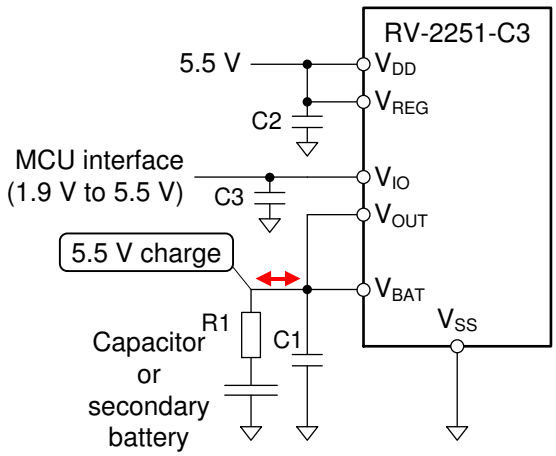
5 Interface lines SCL, SDA and the outputs $\overline{V_{IOL}}$ and $\overline{INT}$ are open drain and require pull-up resistors to V_{IO}.

6 32.768 kHz Clock Output; push-pull. Voltage of high level is equal to V_{IO}. Output always active.

4.1.3.CAPACITOR OR SECONDARY BATTERY 5.5 V CHARGE

Backup with capacitor or secondary battery, 5.5 V charge: Conditions V_{DD}, V_{BAT}, V_{IO}

With capacitor. E.g. electric double layer capacitor (V_{BAT} = 5.5 V).
Charging voltage is more than V_{REG} output voltage.



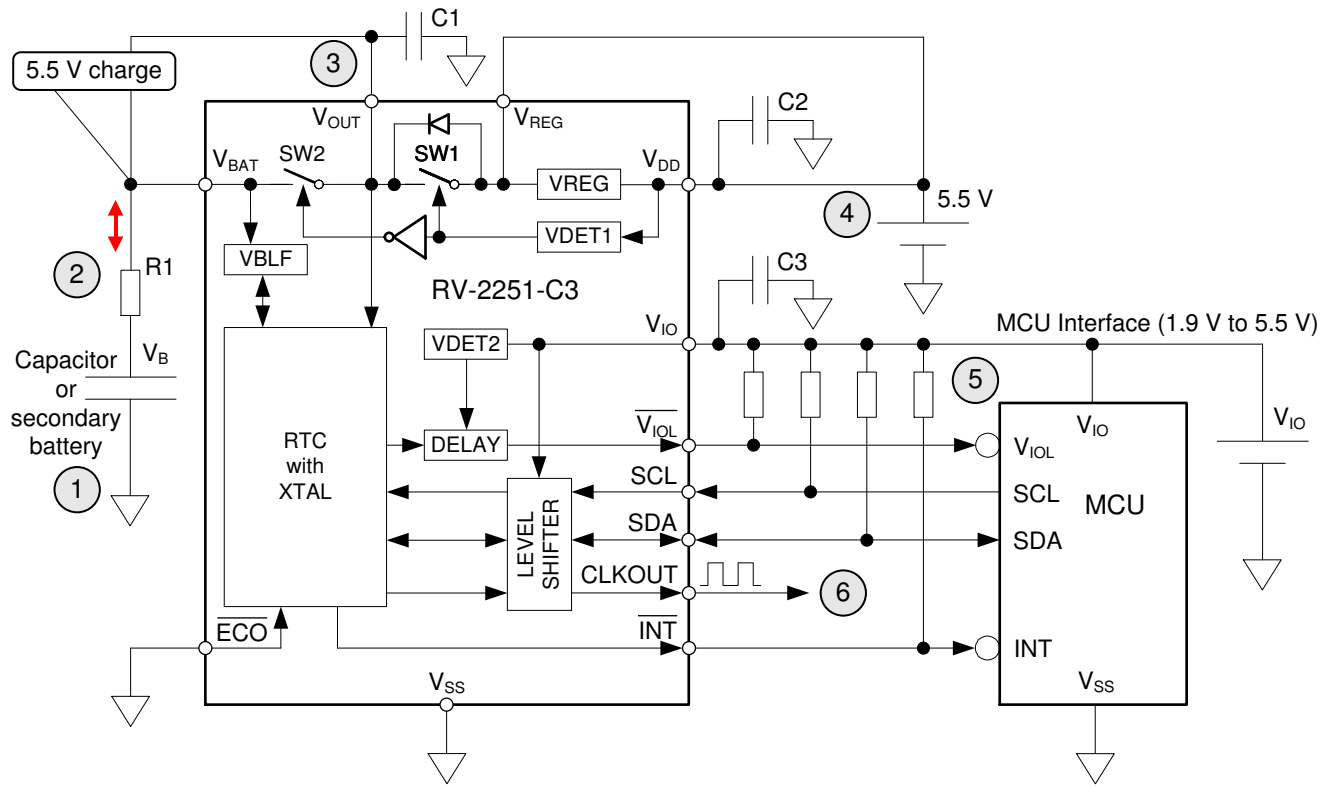
Power state:

- V_{OUT} powered from 0 V to 0.7 V with V_{DD} from 0 V to 1.0 V OR with V_{BAT} from 0 V to 0.7 V
  - POR state
- V_{DD} between 1.0 V and V_{DET1R} (typ. 2.78 V):
  - VBAT Power state
  - Discharging capacitor down to V_{DD}
- V_{DD} between V_{DET1R} (typ. 2.78 V) and 5.5 V:
  - VDD Power state
  - Charging capacitor to V_{DD}

MCU interface access:

- V_{IO} between 0 V and V_{DET2R} (typ. 1.77 V):
  - Interface access disabled
- V_{IO} between V_{DET2R} (typ. 1.77 V) and 5.5 V AND V_{OUT} between 1.0 V and 5.5 V (powered from V_{DD} or V_{BAT}):
  - Interface access enabled

Backup with capacitor or secondary battery, 5.5 V charge: All components



1. Supercapacitor (e.g. 1 farad). Charging voltage is 5.5 V.

2. When using a supercapacitor, a series resistor R1 is used to limit the inrush current into the supercapacitor at power-on. E.g. to comply with the maximum output current of the RV-2251-C3 (I_{Omax} = 10 mA).
To limit the current to comply with the specification of the backup device.
And to fulfill the condition R1 > R_{MCU} * (V_B – (V_{DET1F})) / V_{DET1F}) that after switch off the MCU the voltage V_{DD} is falling below V_{DET1F} for shore and RV-2251-C3 can switch SW1 OFF.

3. A 100 nF decoupling capacitor (C1, C2 and C3) is recommended close to the device for every power supply pin (V_{BAT} with V_{OUT} and V_{REG} with V_{DD} together).

4. Main RTC Power Supply. If the voltage is equal or lower than V_{DET1F}, SW1 is open, and SW2 turns on. As a result, power is supplied from V_{BAT} pin. When V_{DD} is equal or higher than V_{DET1R}, SW1 is closed, and SW2 is opened.

5. Interface lines SCL, SDA and the outputs $\overline{V_{IOL}}$ and $\overline{INT}$ are open drain and require pull-up resistors to V_{IO}.

6. 32.768 kHz Clock Output; push-pull. Voltage of high level is equal to V_{IO}. Output always active.

4.2. POWER-ON RESET

The power-on reset (POR) is generated at start-up when V_{OUT} is powered on from 0 V. The Offset and RAM register are set to 00h and the Control1 and Control2 registers are initialized to their reset values (see REGISTER RESET VALUES SUMMARY). The values of the other registers stay undefined. At the same time, the power on state is stored to dedicated flags, thereby it can be identified whether V_{OUT} was powered on from 0 V (BLF = 1) or if the RV-2251-C3 was backed-up by battery (BLF = 0).

Two conditions can be differentiated:

- The Oscillation Failure Flag OF and the Power-On reset Flag PON confirm the invalidation of time data.
- While the Battery Low Flag BLF indicates only a potential invalidation of time data.

4.3. SUPPLY VOLTAGE MONITORING FUNCTIONS

The V_{DD}, V_{IO} and V_{BAT} pin have their own voltage monitoring functions.

V_{DD} power supply monitoring circuit automatically selects which of the two power supplies, V_{DD} or V_{BAT}, is used for the internal power source V_{OUT}. When V_{DD} voltage is lower than V_{DET1}, V_{BAT} supplies the power to V_{OUT}, and when higher than V_{DET1}, V_{DD} supplies the power to V_{OUT} (see AUTOMATIC BACKUP SWITCHOVER FUNCTION and VDD MONITORING CIRCUIT).
Note that in a circuit where V_{BAT} is not hard-wired to V_{OUT}, the switchover to V_{BAT} (SW2 closed) can only occur after a previous startup of V_{DD}. A voltage V_{DD} of 1.0 V is sufficient, and it can be turned off again after start-up time t_{START}. In such a case, it is not possible to power on from V_{BAT} only (see PRIMARY BATTERY).

V_{IO} peripheral supply monitoring circuit makes $\overline{V_{IOL}}$ pin LOW when V_{IO} peripheral supply pin becomes equal or lower than V_{DET2F}. At the power-on of V_{IO}, this circuit switches off $\overline{V_{IOL}}$ pin (HIGH) after the delay time t_{DELAY} from when the V_{IO} peripheral supply pin becomes equal or more than V_{DET2R} (see VIO MONITORING CIRCUIT).
Note that the V_{IO} monitoring function is only available if V_{OUT} is between 1.0 V and 5.5 V.

V_{BAT} power supply monitoring circuit is equipped with BLF flag in register Control2 that is configured to record any drop in battery supply voltage below the threshold value V_{BLF} (see VBAT MONITORING CIRCUIT).

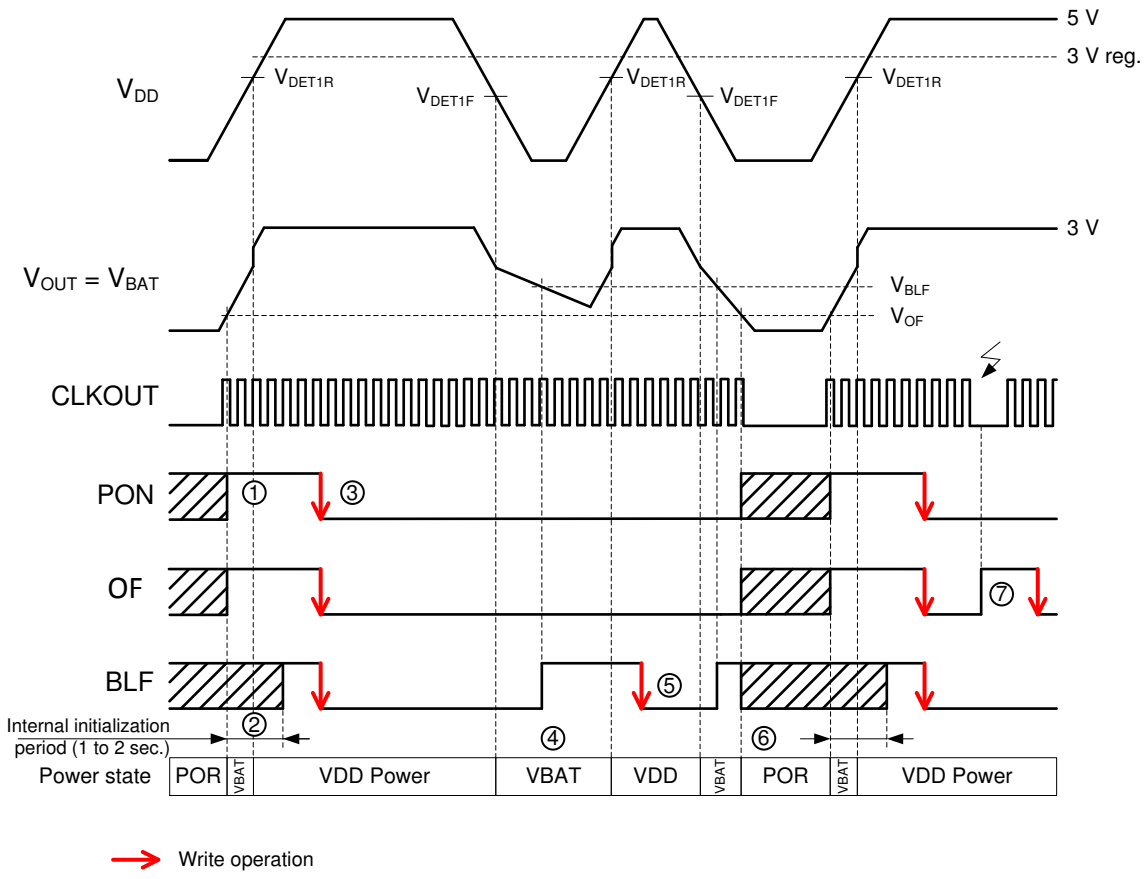
4.3.1. VDD MONITORING CIRCUIT

The V_{DD} supply voltage monitor circuit is part of the automatic backup switchover function and operates always. When V_{DD} rising over V_{DET1R}, SW1 turns on, and SW2 turns off, RTC is in VDD Power state. When V_{DD} is falling beyond V_{DET1F}, SW1 turns off, and SW2 turns on, RTC is in VBAT Power state. In the following example backup is done with a capacitor charged to 3.0 V (see CAPACITOR OR SECONDARY BATTERY 3.0 V CHARGE).

Power states:

VDD Power	SW1 = ON, SW2 = OFF
VBAT Power	SW1 = OFF, SW2 = ON
POR	SW1 = OFF, SW2 = OFF

V_{DD} monitoring:



① The flags PON and OF are set to 1 when V_{OUT} was started from 0 V and the 32.768 kHz oscillator is running.
② The BLF flag is set to 1 and valid after internal initialization period (1 to 2 seconds) doe to sampling V_{BAT}.
③ After the internal initialization period all flags (PON, OF and BLF) can be cleared to 0 by software.
④ The V_{BLF} monitoring circuit detects that V_{BAT} is lower than V_{BLF} and sets the BLF flag to 1.
⑤ When V_{BAT} is over V_{BLF} again the BLF flag can be cleared to 0 by software.
⑥ Once V_{OUT} is not available the RTC is in POR Power state.
⑦ An oscillator failure is indicated by the OF flag although V_{OUT} was assumed to be stable and higher than V_{OF} (can be cleared to 0 by software).

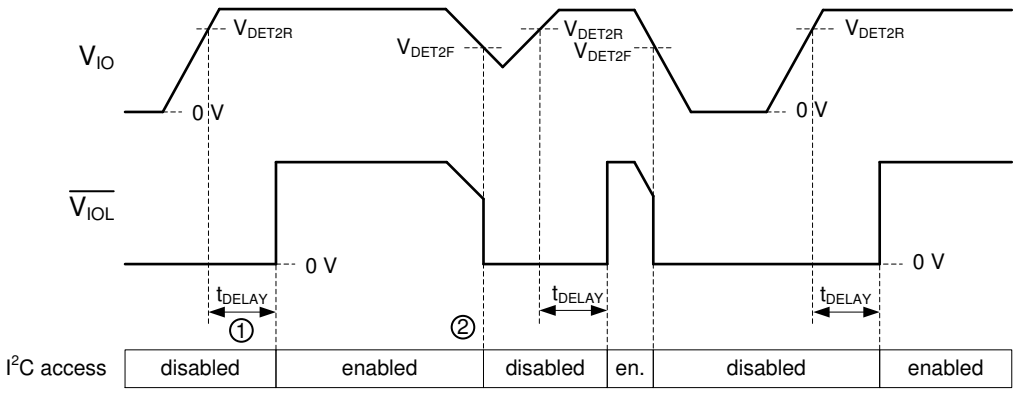
Hint:

- When V_{DD} is rising from 0 V, V_{OUT} follows about the half of V_{DD} voltage level (over SW1 protective diode). Once V_{OUT} has reached V_{OF}, RV-2251-C3 switches to V_{BAT} (SW1 = OFF, SW2 = ON) and V_{OUT} follows V_{BAT}. After V_{DD} rising over V_{DET1R}, V_{OUT} follows V_{DD} voltage level.
- During POR, flags can be read, but the read values are not valid!
- Be aware that the oscillation halt sensing circuit OF will detect also very short voltage drop on V_{OUT} pin:
    - In some cases 1 µF to V_{OUT} pin if needed.

4.3.2.VIO MONITORING CIRCUIT

The $\overline{V_{IOL}}$ is the V_{IO} Peripheral Supply Monitoring Result Output pin that is informing the MCU about the state of the I^2C interface. The V_{IO} supply voltage monitor circuit is always in operation. When V_{IO} is rising over V_{DET2R} and after t_{DELAY}, $\overline{V_{IOL}}$ outputs HIGH and I^2C access is enabled. When V_{IO} falling beyond V_{DET2F}, $\overline{V_{IOL}}$ outputs LOW and the I^2C access is disabled.
Note that the V_{IO} monitoring function is only available if V_{OUT} is between 1.0 V and 5.5 V.

V_{IO} monitoring:



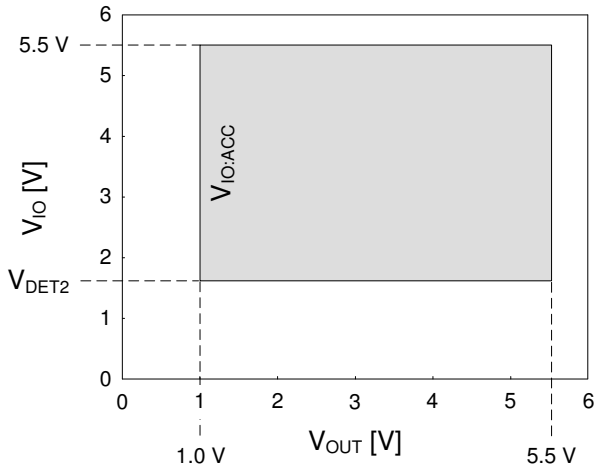
Condition:
V_{OUT} is between 1.0 V and 5.5 V.

① When V_{IO} is higher than V_{DET2R} (typically 1.77 V) and after a typical delay time t_{DELAY} = 105 ms the I^2C access is enabled and $\overline{V_{IOL}}$ is off (HIGH).
② When V_{IO} is lower than V_{DET2F}, I^2C access is disabled immediately and $\overline{V_{IOL}}$ is tied LOW.

4.3.3. VIO LEVEL SHIFTER

Due to the level shifter the MCU interface access using the V_{IO} peripheral supply is independent from the internal supply output voltage V_{OUT} for the RTC in timekeeping mode. The V_{IO} voltage supplies the two I^2C lines and the output pins $\overline{V_{IOL}}$ and $\overline{INT}$ over pull up resistors and the push-pull output pin CLKOUT (32.768 kHz).
Note that the V_{IO} monitoring function is only available if V_{OUT} is between 1.0 V and 5.5 V.

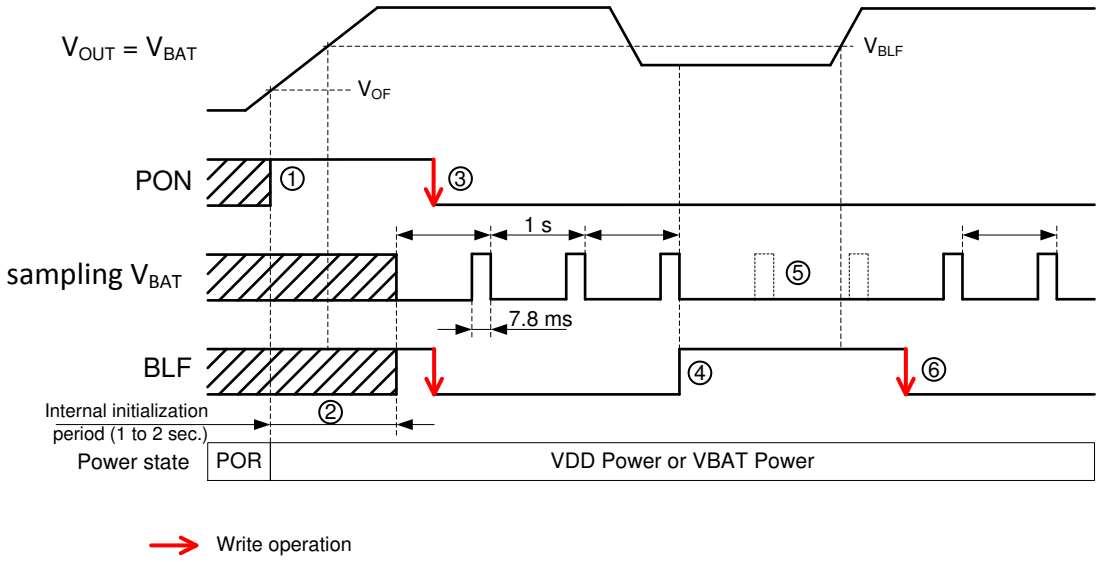
I^2C-bus interface accessibility:



4.3.4.VBAT MONITORING CIRCUIT

The V_{BAT} backup supply voltage monitoring circuit is configured to conduct sampling operation during an interval of 7.8 ms per second to check for a drop in battery supply voltage below a threshold voltage V_{BLF} (typ. = 1.35 V), thus minimizing supply current requirements as illustrated in the timing chart below. This circuit suspends a sampling operation once the BLF flag is set to 1 (register Control2). The V_{BAT} supply voltage monitor is useful for back-up battery checking.

V_{BAT} monitoring:



① The PON flag is set to 1 when V_{OUT} was started from 0 V and the 32.768 kHz oscillator is running.
② The BLF flag is set to 1 and valid after internal initialization period (1 to 2 seconds) doe to sampling V_{BAT}.
③ After the internal initialization period both flags (PON and BLF) can be cleared to 0 by software.
④ The backup monitoring circuit detects that V_{BAT} is lower than V_{BLF} and sets the BLF flag to 1.
⑤ As long as BLF is set, V_{BAT} is not sampled by the monitoring circuit to minimize supply current.
⑥ After the BLF flag is cleared to 0 by software the monitoring circuit begins with sampling V_{BAT} again.

Hint:
During the interval of 7.8 ms the typical current sensing peak is $I_{VBAT:VSP}$ = 900 nA. The typical I_{VBAT} average current when V_{BAT} is sampled can be calculated as follows:

$$I_{VBAT\_Average} = ((I_{VBAT:VSP} * 7.8\ ms) + (I_{VBAT\_Sampling\ OFF} * (1\ s - 7.8\ ms))) / 1\ s$$

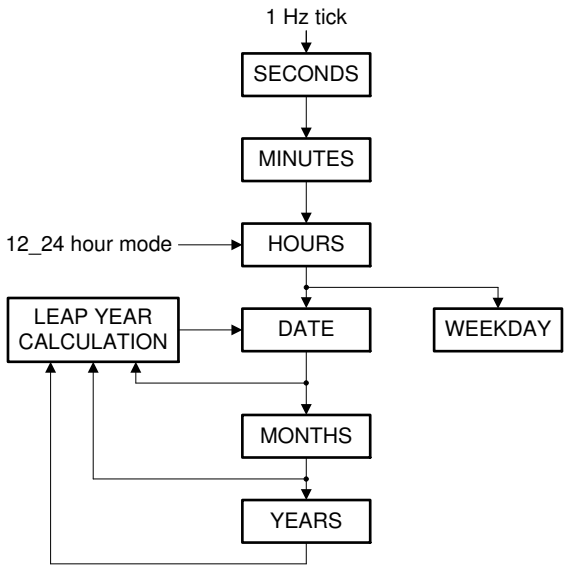
$$= ((900\ nA * 7.8\ ms) + (210\ nA * 992.2\ ms)) / 1\ s$$

$$= \underline{215\ nA}$$

4.4. RTC COUNTER ACCESS

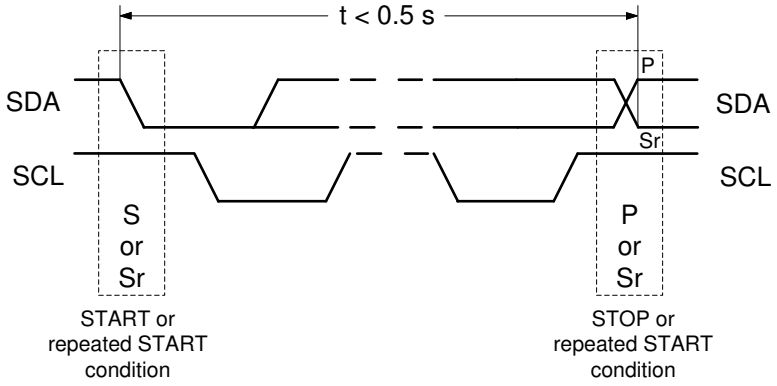
The following Figure shows the data flow and data dependencies starting from the 1 Hz clock tick.

Data flow for the time function:



Caution:
When one of the RTC registers is written or read, the contents of all time counters are frozen for up to 0.5 second. To guarantee that either read or write timer value is consistent, a single burst should be limited to < 0.5 seconds. Therefore, when communicating with the RV-2251-C3 module, the series of operations from transmitting the START (or repeated START) condition to transmitting the STOP (or repeated START) condition should occur within 0.5 second. If this series of operations requires 0.5 second or more, the I^2C bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-2251-C3 module.
Note with caution that both write and read operations have to be regarded as invalid when occurred during or after this auto clearing operation.
Restarting of communications begins with transfer of the START condition again.

Access time for read/write operations:

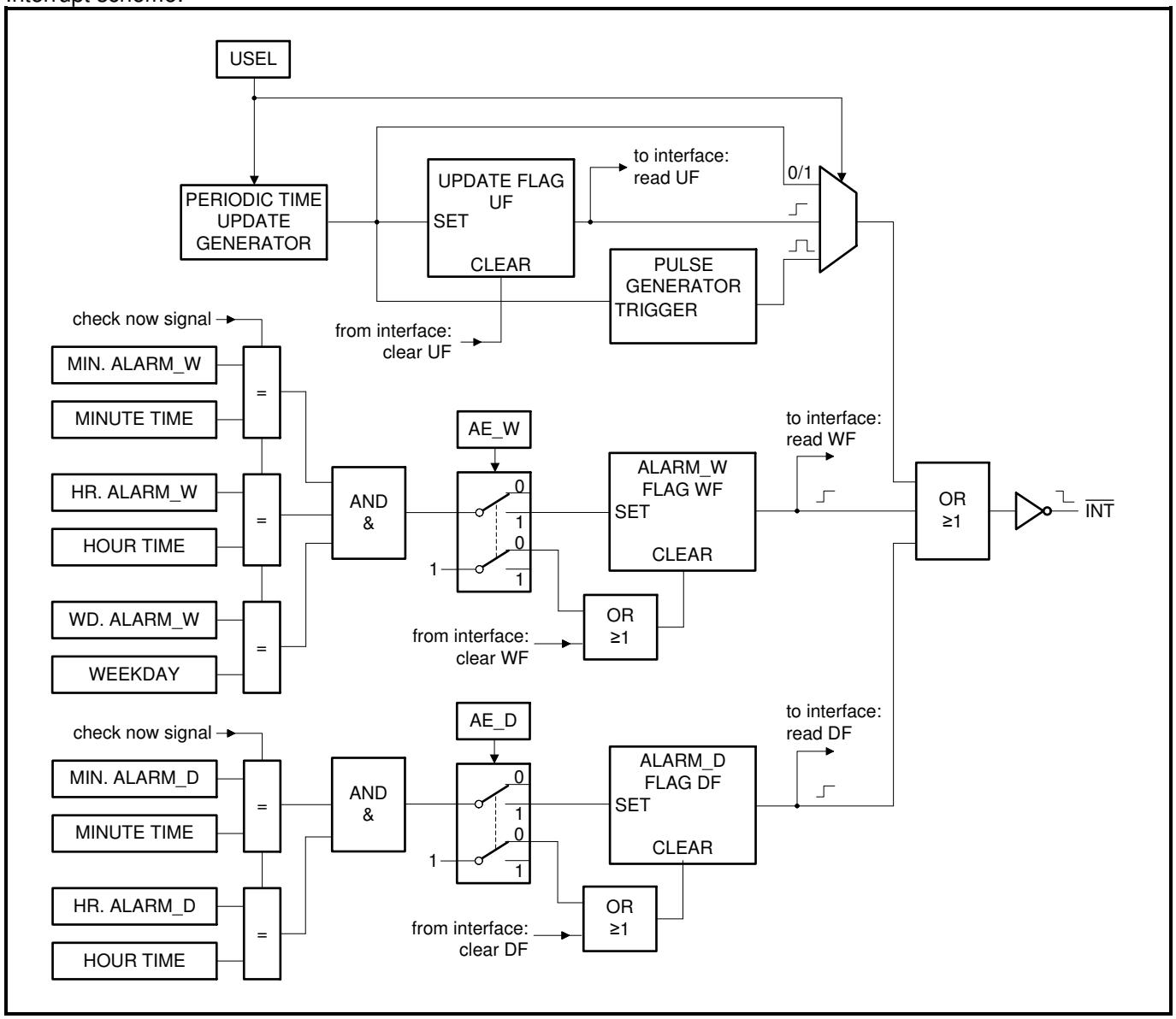


4.5. INTERRUPT SUMMARY

The interrupt pin $\overline{INT}$ can be triggered by the Periodic Time Update Interrupt signal and by the Alarm_W and Alarm_D signals:

- PERIODIC TIME UPDATE INTERRUPT FUNCTION
- ALARM FUNCTIONS

Interrupt scheme:



4.6. PERIODIC TIME UPDATE INTERRUPT FUNCTION

The RV-2251-C3 incorporates the Periodic Time Update Interrupt circuit configured to generate periodic interrupt signals on pin $\overline{INT}$. In the Pulse Mode the frequencies of 2 Hz and 1 Hz can be selected. In Level Mode the frequencies of 1 Hz, 1/60 Hz (once per 1 minute), 1/3600 Hz (once per 1 hour), and monthly (the first day of every month) can be selected. The condition of periodic time update interrupt signals can be monitored by reading (polling) the update flag UF (see CONTROL REGISTERS, Fh – Control2).

Periodic Time Update Interrupt selection field USEL:

USEL	USEL-Mode	$\overline{INT}$ Frequency
000	-	OFF ($\overline{INT}$ = HIGH) – Default value
001	-	Always ON ($\overline{INT}$ = LOW) (1)
010	Pulse	2 Hz (2) (3)
011	Pulse	1 Hz (2) (3)
100	Level	Every second (3)
101	Level	Every minute
110	Level	Every hour
111	Level	Every month

(1) When USEL = 001b the flag UF cannot be reset to 0.
(2) Duty cycle = 50%
(3) In Pulse Mode the 2 Hz and 1 Hz clock pulses and in Level Mode the 1 Hz signal can be affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

When the offset adjustment is used, the interrupt cycle will fluctuate once per 20 seconds or 60 seconds as follows:

- Pulse Mode: The HIGH period of the $\overline{INT}$ output pulses will increment or decrement by a maximum of ±3.784 ms. For example, 1-Hz clock pulses will have a duty cycle of 50 ±0.3784%.
- Level Mode: A periodic time update interrupt of 1 second will increment or decrement by a maximum of ±3.784 ms.

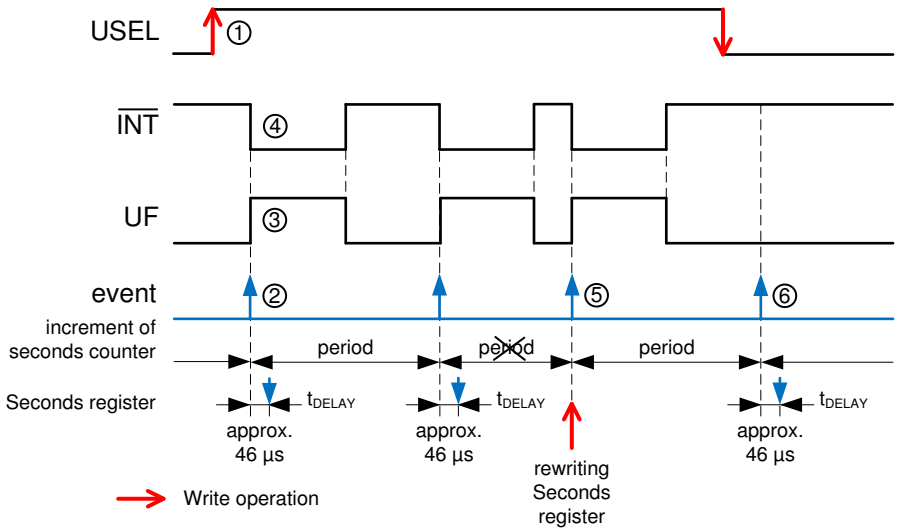
Hint:
Maximum correction once per 20 seconds or 60 seconds:

- Offset Mode = 0 (maximum range = ±189 ppm): → 20 s * ±189 ppm = ±3.784 ms
- Offset Mode = 1 (maximum range = ±63 ppm): → 60 s * ±63 ppm = ±3.784 ms

4.6.1.PULSE MODE

Pulse Mode: 2-Hz and 1-Hz clock pulses are outputted in synchronization with the increment of the seconds counter as illustrated in the timing chart below.

Diagram of the Periodic Time Update Interrupt function in Pulse Mode (example with 1 Hz):



① Set USEL field to 010b or 011b to enable 2-Hz respective 1-Hz periodic time update interrupt function in pulse mode.
② A Periodic Time Update Interrupt event occurs when the internal clock value matches either the seconds or 0.5 seconds update time. Note, that the increment of the Seconds register is delayed be approximately 46 µs.
③ When a Periodic Time Update Interrupt occurs, the UF bit is set to 1.
④ If the USEL field is in pulse mode and a Periodic Time Update Interrupt occurs, the $\overline{INT}$ pin output goes low.
⑤ Rewriting the seconds counter will reset the other time counters of less than 1 second, driving the $\overline{INT}$ pin low.
⑥ If the USEL field value is set to 000b, the $\overline{INT}$ pin is disabled (stay/goes HIGH).

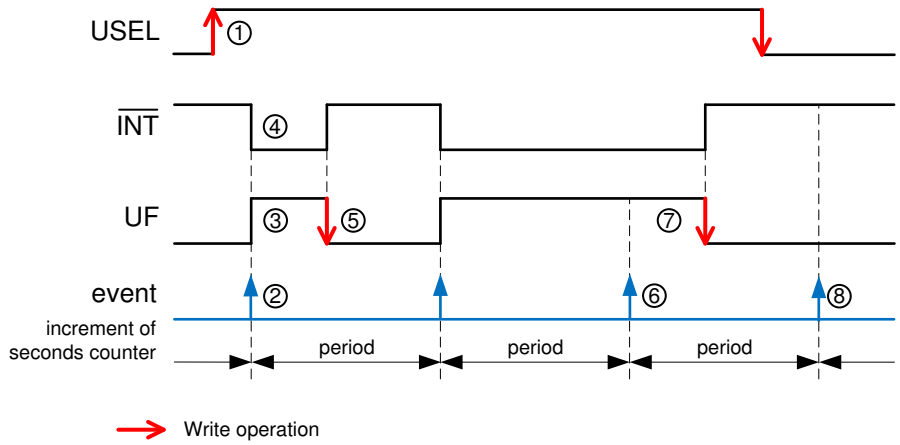
In the pulse mode, the increment of the Seconds register value is delayed by approximately 46 µs from the falling edge of $\overline{INT}$ pulses. Consequently, time readings immediately after the falling edge of the $\overline{INT}$ pulses may appear with a lag of 1 second behind the real-time counts. Rewriting the seconds counter will reset the other time counters of less than 1 second, driving the $\overline{INT}$ pin low.

Note:
In Pulse Mode the 2 Hz and 1 Hz clock pulses can be affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

4.6.2.LEVEL MODE

Level Mode: Periodic Time Update Interrupt signals are output with selectable interrupt cycle settings of 1 second, 1 minute, 1 hour, and 1 month. The increment of the seconds counter is synchronized with the falling edge of periodic interrupt signals. For example, periodic interrupt signals with an interrupt cycle setting of 1 second are output in synchronization with the increment of the seconds counter as illustrated in the timing chart below.

Diagram of the Periodic Time Update Interrupt function in Level Mode:



① Set USEL field to 100b, 101b, 110b or 111b to enable second, minute, hour or monthly Periodic Time Update Interrupt function in level mode. Note, that the moment right after writing to USEL, $\overline{INT}$ pin can become LOW in a very short time. In such a case, ignore it or confirm it by clearing UF flag.

② A Periodic Time Update Interrupt event occurs when the internal clock value matches either seconds, minutes, hours or month update time.

③ When a Periodic Time Update Interrupt occurs, the UF bit is set to 1.

④ When UF bit is set, the $\overline{INT}$ pin output goes low.

⑤ If the $\overline{INT}$ pin is low, its status changes as soon as the UF flag is cleared from 1 to 0.

⑥ No interrupt occurs because the UF flag was not set back to 0.

⑦ The UF flag retains 1 until it is cleared to 0 by software.

⑧ If the USEL field value is set to 000b, the $\overline{INT}$ pin is disabled (stay/goes HIGH).

Note:
In Level Mode the 1 Hz signal can be affected by compensation pulses (see FREQUENCY OFFSET COMPENSATION).

4.6.3.USE OF THE PERIODIC TIME UPDATE INTERRUPT

Field and bit related to the Periodic Time Update Interrupt function:

- USEL field (see CONTROL REGISTERS, Eh - Control1)
- UF bit (see (see CONTROL REGISTERS, Fh – Control2)

Prior to entering any other settings, it is recommended to write a 000b to the USEL field to prevent inadvertent interrupts on $\overline{\text{INT}}$ pin.

Procedure to use the Periodic Time Update Interrupt function:

1. Initialize field USEL to 000b and bit UF to 0.
2. Choose and enable the frequency and mode by writing the corresponding value to the USEL field.
    a. In Pulse Mode the first interrupt occurs when the internal clock value matches either the seconds or the 0.5 seconds update time.
    b. In Level Mode the first interrupt occurs when the internal clock value matches either seconds, minutes, hours or month update time. Confirm it by writing 0 to the UF flag to be prepared for a next event.

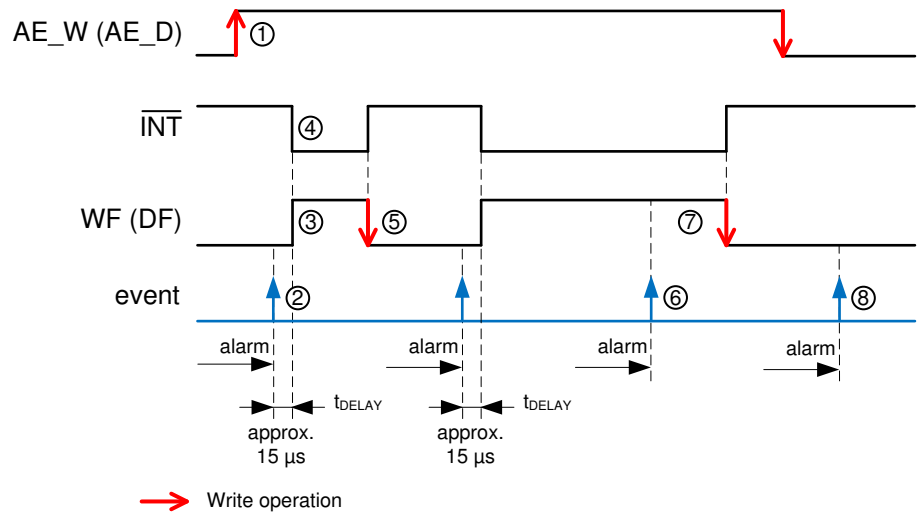
4.7. ALARM FUNCTIONS

The RV-2251-C3 incorporates the Alarm Interrupt circuit configured to generate interrupt signals to the MCU at preset times. The Alarm Interrupt circuit allows two types of alarm settings specified by the Alarm_W registers (pointers 8h, 9h and Ah, see ALARM_W REGISTERS) and the Alarm_D registers (pointers Bh and Ch, see ALARM_D REGISTERS). The Alarm_W registers allow weekdays, hours, and minutes alarm settings including combinations of multiple weekday settings such as Monday, Wednesday and Friday, Saturday and Sunday. The Alarm_D registers allow hour and minute alarm settings. The Alarms output to $\overline{INT}$ pin. Each alarm function can be checked from the MCU by reading (polling) the alarm flags WF and DF (see CONTROL REGISTERS, Fh – Control2). When the comparisons first match, the flags are set logic 1.

- The $\overline{INT}$ pin always follows the conditions of the flags WF and DF linked with logic OR.
- The WF and DF flags accept only the writing of 0.
- If the bits AE_W and AE_D are set to 1 the WF and DF flags indicate alarm events. The events are generated approximately 15 µs after any match between current time and preset alarm time specified by the Alarm_W and Alarm_D registers. Once WF and DF have been cleared, they will only be set again when the time increments to match an alarm condition once more.
- If the bits AE_W and AE_D are reset to 0 the alarm interrupt circuits are disabled and the flags WF and DF always read out 0 (see following ALARM DIAGRAM).

4.7.1.ALARM DIAGRAM

Diagram of the Alarm Interrupt functions:



① Set AE_W (AE_D) to 1 to enable the corresponding Alarm Interrupt function.
② An Alarm Interrupt event occurs when the selected Alarm registers match the respective counters.
③ When an Alarm Interrupt event occurs, the WF (DF) flag is set to 1.
④ If the AE_W (AE_D) bit is 1 and an Alarm Interrupt occurs, the $\overline{INT}$ pin output goes low.
⑤ If the $\overline{INT}$ pin is low, its status changes as soon as the WF (DF) flag is cleared from 1 to 0.
⑥ No interrupt occurs because the WF (DF) flag was not set back to 0.
⑦ The WF (DF) flag retains 1 until it is cleared to 0 by software.
⑧ If the AE_W (AE_D) bit value is 0 when an Alarm event occurs, the $\overline{INT}$ pin status does not go low.

4.7.2.USE OF THE ALARM INTERRUPTS

Registers and bits related to the two Alarm Interrupt functions Alarm_W and Alarm_D:

Alarm_W:
- Minutes Register (1h) (see TIME AND DATE REGISTERS)
- Hours Register (2h) (see TIME AND DATE REGISTERS)
- Weekday Register (3h) (see TIME AND DATE REGISTERS)
- Alarm_W Minutes (8h) (see ALARM_W REGISTERS)
- Alarm_W Hours (9h) (see ALARM_W REGISTERS)
- Alarm_W Weekdays (Ah) (see ALARM_W REGISTERS)
- AE_W bit (see CONTROL REGISTERS, Eh - Control1)
- WF flag (see (see CONTROL REGISTERS, Fh – Control2)

Alarm_D:
- Minutes Register (1h) (see TIME AND DATE REGISTERS)
- Hours Register (2h) (see TIME AND DATE REGISTERS)
- Alarm_D Minutes (Bh) (see ALARM_D REGISTERS)
- Alarm_D Hours (Ch) (see ALARM_D REGISTERS)
- AE_D bit (see CONTROL REGISTERS, Eh - Control1)
- DF flag (see (see CONTROL REGISTERS, Fh – Control2)

Prior to entering any timer settings for an Alarm Interrupt, it is recommended to write a 0 to the AE_W (AE_D) bit to prevent inadvertent interrupts on $\overline{INT}$ pin.

Procedure to use the Alarm Interrupt functions:
1. Initialize bit AE_W (AE_D) and flag WF (DF) to 0.
2. Write the desired alarm settings in registers with pointers 8h, 9h and Ah (Bh and Ch).
3. Set the AE_W (AE_D) bit to 1 to enable the corresponding Alarm Interrupt function.

4.8. SERVICING INTERRUPTS

The $\overline{INT}$ pin can indicate three types of interrupts. It outputs the logic OR operation result of these interrupt outputs. When an interrupt is detected, (when the $\overline{INT}$ pin is at low level), the UF, WF and DF flags can be read to determine which interrupt event has occurred.
The $\overline{INT}$ pin is always connected to the OR'ed flag signals and cannot be disconnected separately. To check whether an event has occurred without monitoring the $\overline{INT}$ pin, software can read the UF, WF and DF interrupt flags (polling).

4.9. FREQUENCY OFFSET COMPENSATION

The RV-2251-C3 incorporates an Offset register (see OFFSET REGISTER, 7h – Offset Register) which can be used by customer to compensate the frequency offset of the 32.768 kHz oscillator which allows implementing functions, such as:

- Improve time accuracy
- Aging compensation

7h – Offset Register:

Address Pointer	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7h	Offset	MODE	OFFSET						
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	MODE		Offset Mode
		0	Normal Mode: Offset is compensated every 20 seconds (at 00, 20 and 40).
		1	Slow Mode: Offset is compensated every minute (at seconds = 00).
6:0	OFFSET	-62 to +62	Defines compensation pulses in steps. For MODE = 0, each pulse introduces a deviation of 3.052 ppm, the maximum range is ±189 ppm. For MODE = 1, each pulse introduces a deviation of 1.017 ppm, the maximum range is ±63 ppm. The values of 3.052 ppm and 1.017 ppm are based on a nominal 32.768 kHz clock (see FREQUENCY OFFSET COMPENSATION).

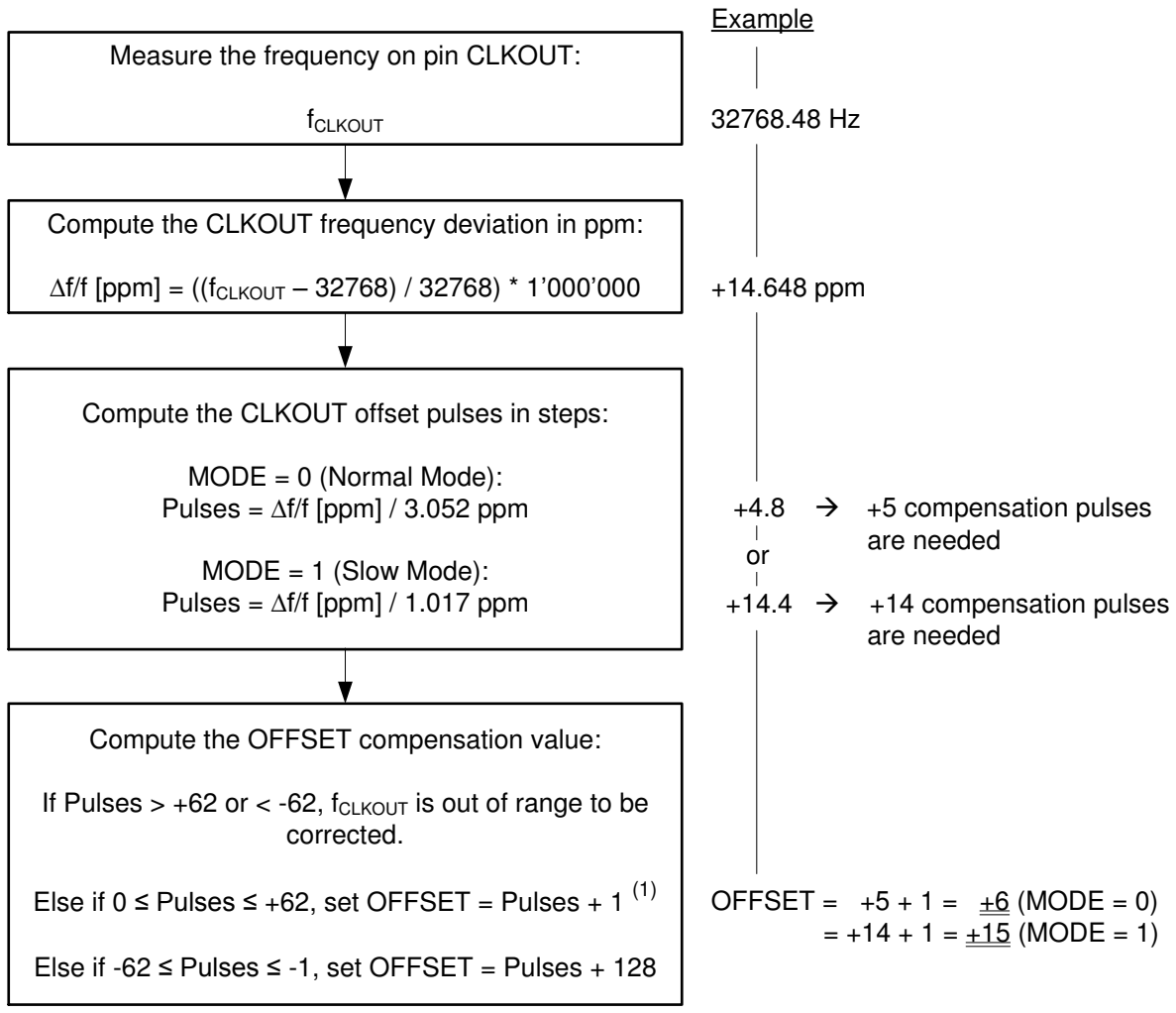
OFFSET	OFFSET compensation value in decimal	Converting (mathematical operation)	Compensation pulses in steps	CLKOUT frequency deviation in ppm[2]	
				Normal Mode MODE = 0	Slow Mode MODE = 1
0111111	+63	-1	+62	+189.209	+63.070
0111110	+62	-1	+61	+186.157	+62.052
:	:	:	:	:	:
0000011	+3	-1	+2	+6.104	+2.035
0000010	+2	-1	+1	+3.052	+1.017
0000001 [1]	+1	×0	0	0	0
0000000 [1]	0				
1111111	+127	Two's complement	-1	-3.052	-1.017
1111110	+126	Two's complement	-2	-6.104	-2.035
:	:	:	:	:	:
1000011	+67	Two's complement	-61	-186.157	-62.052
1000010	+66	Two's complement	-62	-189.209	-63.070
1000001 [1]	+65	×0	0	0	0
1000000 [1]	+64				

[1] The OFFSET values X00000X mean no correction steps are done (X representing 0 or 1) and the offset circuit is disabled. With this converting method a symmetrical structure of ±62 correction steps can be guaranteed.

[2] For MODE = 0, each compensation pulse corresponds to 1/(32768×10) = 3.052 ppm. For MODE = 1 it is 1/(32768×30) = 1.017 ppm. The frequency deviation measured at CLKOUT pin can be compensated by computing the compensation value OFFSET and writing it into the Offset register (see OFFSET COMPENSATION CALCULATION WORKFLOW).

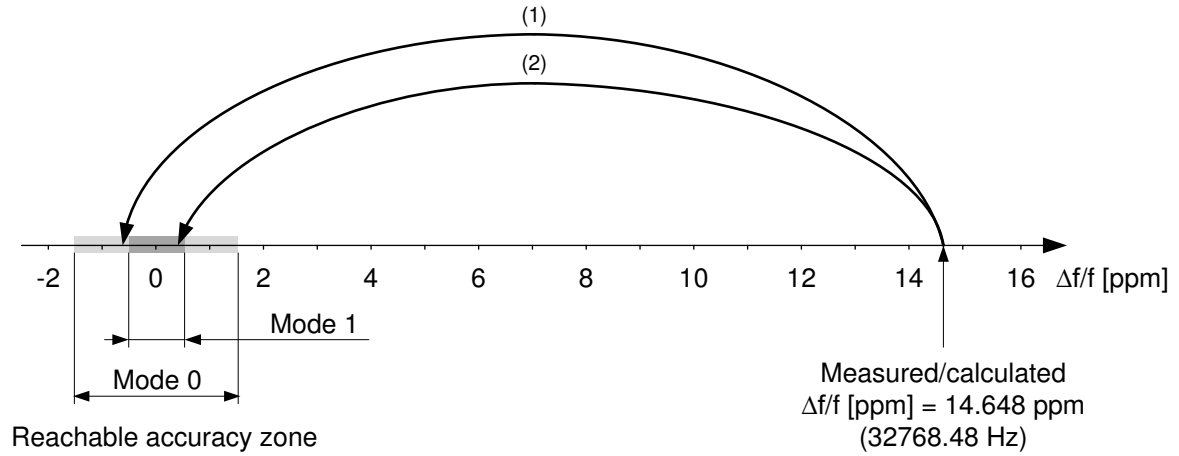
4.9.1.OFFSET COMPENSATION CALCULATION WORKFLOW

Offset compensation calculation workflow:



(1) See table column 'Converting (mathematical operation)' in section FREQUENCY OFFSET COMPENSATION.

Result of the offset compensation (Example):



With the offset compensation the accuracy of ±1.53 ppm (Mode 0) and ±0.51 ppm (Mode 1) (0.5 * offset per puls) can be reached (see OFFSET REGISTER).

- ±1.53 ppm corresponds to a time deviation of 0.132 seconds per day.
- ±0.51 ppm corresponds to a time deviation of 0.044 seconds per day.

(1) MODE = 0: Deviation after compensation = Δf/f [ppm] – compensation pulses * 3.052 ppm
= 14.648 ppm – 5 * 3.052 ppm = -0.61 ppm

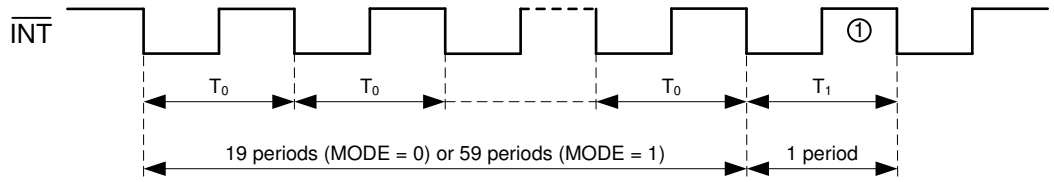
(2) MODE = 1: Deviation after compensation = Δf/f [ppm] – compensation pulses * 1.017 ppm
= 14.648 ppm – 14 * 1.017 ppm = +0.41 ppm

4.9.2.MEASURING TIME ACCURACY AT $\overline{INT}$ PIN

The offset circuit is configured to change time counts of 1 second on the basis of the settings of the Offset register once in 20 seconds or 60 seconds. The offset circuit does not affect the frequency of 32.768 kHz-clock pulse output from the CLKOUT pin. Therefore, after writing the Offset register, the clock deviation cannot be measured with probing CLKOUT clock pulses. The way to measure the clock deviation is the following:

1. Select the Periodic Time Update Interrupt function with the frequency 1 Hz in Pulse Mode at the $\overline{INT}$ output pin:
   a. Initialize field USEL to 000b and bit UF to 0.
   b. Choose and enable the frequency of 1 Hz in Pulse Mode by writing 011b to USEL.
   c. The first interrupt occurs when the internal clock value matches the seconds update time.
2. After setting the Offset register, the 1Hz clock period changes every 20 seconds (or every 60 seconds) as shown below.

1 Hz clock pulse on $\overline{INT}$ pin:



① The HIGH level of the T_1 pulse will increment or decrement by a maximum of ±3.784 ms.

3. Measure the T_0 and T_1 periods with a high-precision universal counter on $\overline{INT}$ output pin.
4. Calculate the average period T_{AVER} to receive the time accuracy:
   a. When MODE = 0:
      $T_{AVER} = (19 * T_0 + 1 * T_1) / 20$ s
   b. When MODE = 1:
      $T_{AVER} = (59 * T_0 + 1 * T_1) / 60$ s
5. Calculate the new achieved frequency offset:

$$\text{Frequency offset [ppm]} = \left(\frac{1}{T_{AVER}} - 1\right) * 1'000'000$$

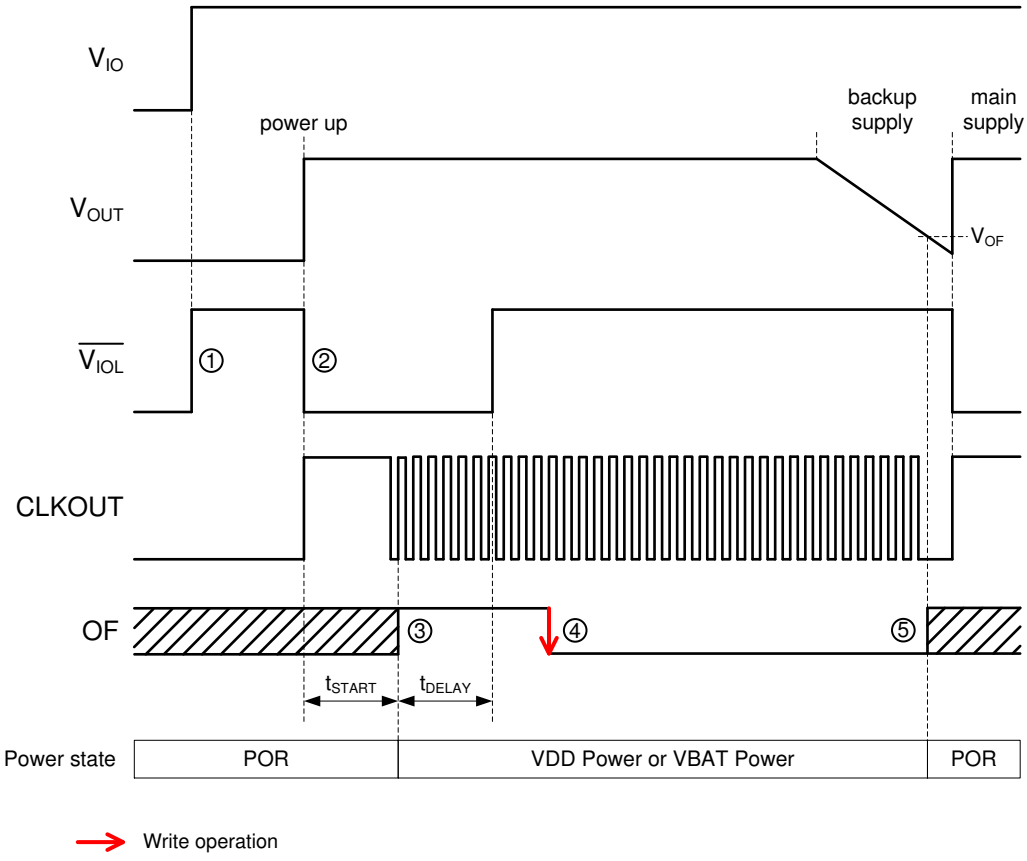
Note:
If following three conditions are true, the actual offset value could be different from the target offset value that is set in the Offset register:
1. Offset function is used.
2. I^2C read access to RV-2251-C3 at random, or synchronized with external clock that has no relation to RV-2251-C3, or synchronized with Periodic Time Update Interrupt in pulse mode.
3. Access to RV-2251-C3 more than two times per each second on average.

4.10. OSCILLATOR FAILURE DETECTION

When the oscillator of the RV-2251-C3 is stopped, the Oscillator failure flag OF is set. The oscillator is considered to be stopped between power up and stable crystal oscillation (start-up time t_{START}). This time can be in a range of typical 100 ms to maximal 500 ms depending on temperature and supply voltage.

The flag remains set until cleared by command (see following Figure). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

OF flag:



① $\overline{V_{IOL}}$ goes HIGH but is not yet valid since V_{OUT} is still 0 V.

② At power up of V_{OUT}, $\overline{V_{IOL}}$ is tied low and indicating POR during the time $t_{START} + t_{DELAY}$ (typically 100 ms + 105 ms = 205 ms).

③ After t_{START} the oscillation is stable and the flags OF (and POR) can be read, but the read values are not valid.

④ After $t_{START} + t_{DELAY}$ the flags are valid and can be cleared to 0 by software.

⑤ When V_{OUT} is lower than V_{OF}, the oscillator is stopped and RV-2251-C3 is again in POR power state.

4.11. 32-KHZ CLOCK OUTPUT

The RV-2251-C3 includes a crystal oscillator which runs at 32.768 kHz. This frequency is always output to the CLKOUT pin (CMOS push-pull) and the high level of the signal is equal to the V_{IO} voltage.

4.12. ECO MODE

The ECO mode permits to lower the power consumption. When the ECO mode is activated ($\overline{ECO}$ pin is tied to Ground) the timekeeping current consumption (in V_{DD} and V_{BAT} mode) is reduced and the oscillation frequency might change slightly. The full time accuracy is guaranteed for the temperature range of 0 to 50°C.

If the ECO mode is deactivated ($\overline{ECO}$ is HIGH) the timekeeping current is little increased and the full time accuracy is guaranteed over the complete temperature and voltage range.

Applications:

- $\overline{ECO}$ pin tied to Ground: The RV-2251-C3 is permanently in ECO mode.
- $\overline{ECO}$ pin connected to V_{OUT}: The RV-2251-C3 is permanently in Non-ECO mode.
- $\overline{ECO}$ pin connected to V_{DD}: The RV-2251-C3 is changing from Non-ECO to ECO mode when V_{DD} is shutting down and the RV-2251-C3 is supplied from V_{BAT}. Depending of the circuitry a pull down resistor (100 kΩ) for $\overline{ECO}$ pin may be needed.

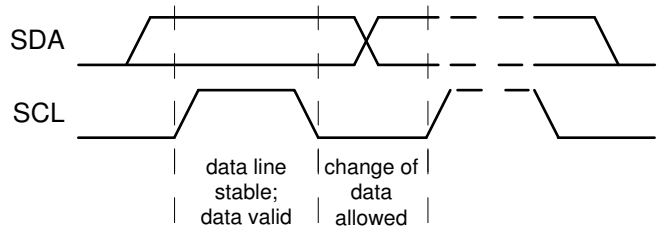
5. I²C-BUS INTERFACE

The I²C interface is for bidirectional, two-line communication between different ICs or modules. The RV-2251-C3 is accessed at addresses 64h/65h, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are open drain and connected to the positive peripheral supply V_{IO} via pull-up resistors. Data transfer is initiated only when the interface is not busy. When V_{IO} is lower than V_{DET2F}, access is disabled.

5.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see Figure below).

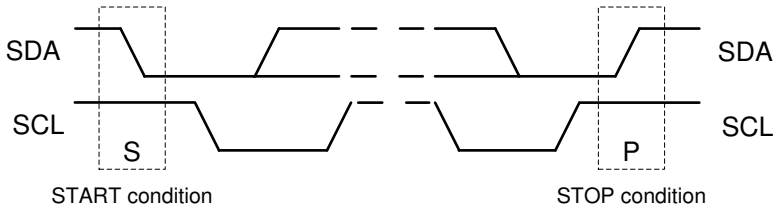
Bit transfer:



5.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure below).

Definition of START and STOP conditions:



A START condition which occurs after a previous START but before a STOP is called a Repeated START condition.

Hint:
To realize a Repeated START condition with RV-2251-C3, do not insert a STOP before a START condition; otherwise the Address Pointer is automatically set to Fh.

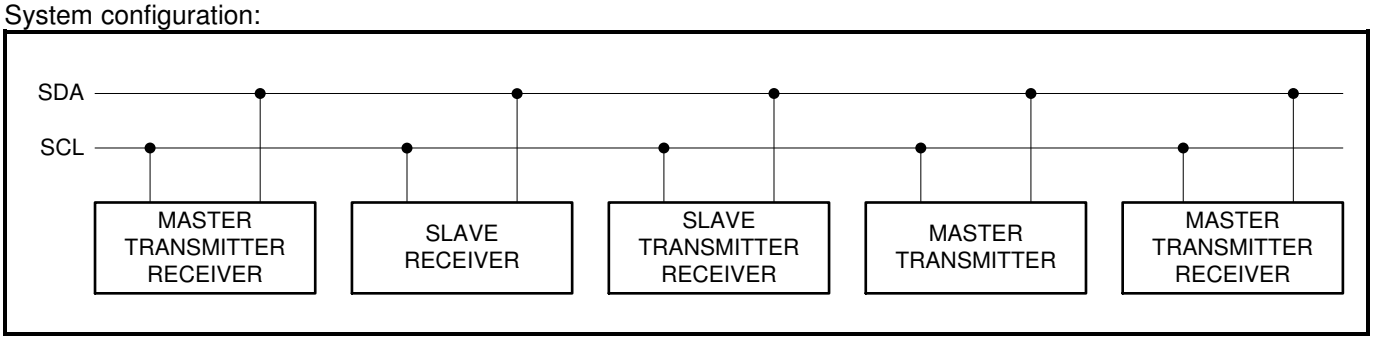
5.3. DATA VALID

After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited. The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

5.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I^2C bus, all I^2C bus devices have a fixed and unique device address built-in to allow individual addressing of each device.
The device that controls the I^2C bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-2251-C3 acts as a Slave-Receiver or Slave-Transmitter.
Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal and only generated by a Master, but the data signal SDA is a bidirectional line.

System configuration:

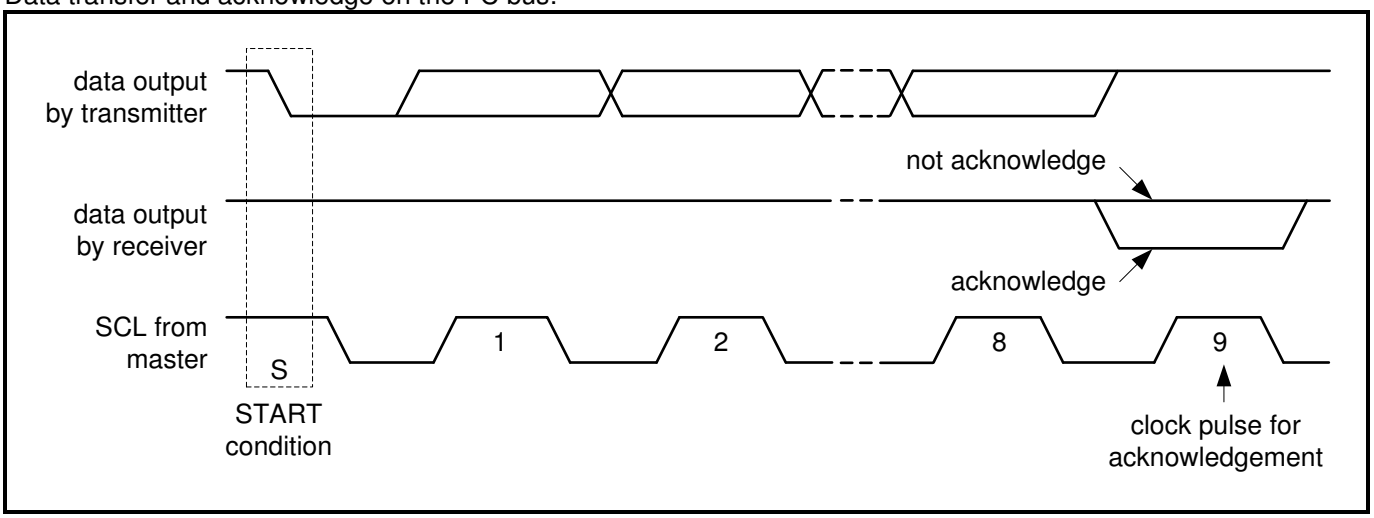


5.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I^2C bus:



5.6. SLAVE ADDRESS

On the I^2C-bus the 7-bit slave address 0110010b is reserved for the RV-2251-C3. The entire I^2C-bus slave address byte is shown in the following table.

Slave address							R/$\overline{W}$	Transfer data
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	1	1	0	0	1	0	1 (R)	65h (read)
							0 ($\overline{W}$)	64h (write)

After a START condition, the I^2C-bus slave address has to be sent to the RV-2251-C3 device. The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 0110010b, the RV-2251-C3 is selected, the eighth bit indicates a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) operation (results in 65h or 64h) and the RV-2251-C3 supplies the ACK. The RV-2251-C3 ignores all other address values and does not respond with an ACK.
In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

5.7. REGISTER ADDRESS

The 8-bit Register Address value that defines which register is to be accessed next is a combination of the 4-bit Address Pointer and the 4-bit Transmission Format.

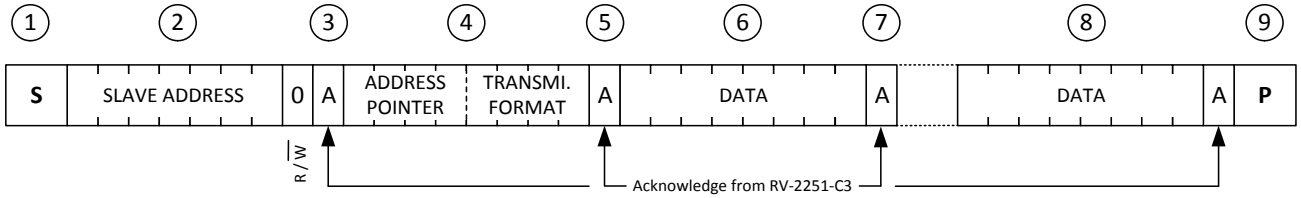
Address Pointer				Transmission Format				Usage
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0h to Fh				0	0	0	0	The Transmission Format is always 0000b (see WRITE OPERATION and NORMAL READ AT SPECIFIC ADDRESS)
				0	1	0	0	The Transmission Format is 0100b or 0101b. Both values are equivalent (see POWER SAVING READ AT SPECIFIC ADDRESS)
				0	1	0	1	

5.8. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The 8-bit Register Address value that defines which register is to be accessed next is a combination of the 4-bit Address Pointer and the 4-bit Transmission Format. For the write operation the Transmission Format must always be 0000b. After writing one byte, the Address Pointer is automatically incremented by 1.

Master writes to slave RV-2251-C3 at specific address:

1) Master sends out the START condition.
2) Master sends out Slave Address, 64h for the RV-2251-C3; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-2251-C3.
4) Master sends out the 4-bit Address Pointer and the 4-bit Transmission Format to RV-2251-C3.
   For the write operation the Transmission Format must always be 0000b.
5) Acknowledgement from RV-2251-C3.
6) Master sends out the Data to write to the specified address in step 4).
7) Acknowledgement from RV-2251-C3.
8) Steps 6) and 7) can be repeated if necessary.
   The Address Pointer is automatically incremented in the RV-2251-C3.
9) Master sends out the STOP Condition.

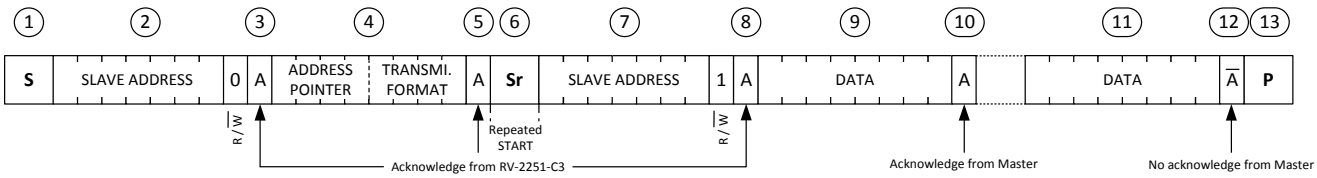


5.9. READ OPERATION

5.9.1.NORMAL READ AT SPECIFIC ADDRESS

Master reads data from slave RV-2251-C3 at specific address:

1) Master sends out the START condition.
2) Master sends out Slave Address, 64h for the RV-2251-C3; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-2251-C3.
4) Master sends out the 4-bit Address Pointer and the 4-bit Transmission Format to RV-2251-C3.
   For the normal write operation the Transmission Format must always be 0000b.
5) Acknowledgement from RV-2251-C3.
6) Master sends out the Repeated START condition. Do not insert a STOP before a START condition; otherwise the Address Pointer is automatically set to Fh.
7) Master sends out Slave Address, 65h for the RV-2251-C3; the R/$\overline{W}$ bit is a 1 indicating a read operation.
8) Acknowledgement from RV-2251-C3.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
9) The Slave sends out the Data from the Address specified in step 4).
10) Acknowledgement from Master.
11) Steps 9) and 10) can be repeated if necessary.
    The Address Pointer is automatically incremented in the RV-2251-C3.
12) The Master, addressed as Receiver, can stop data transmission by not generating acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
13) Master sends out the STOP condition.

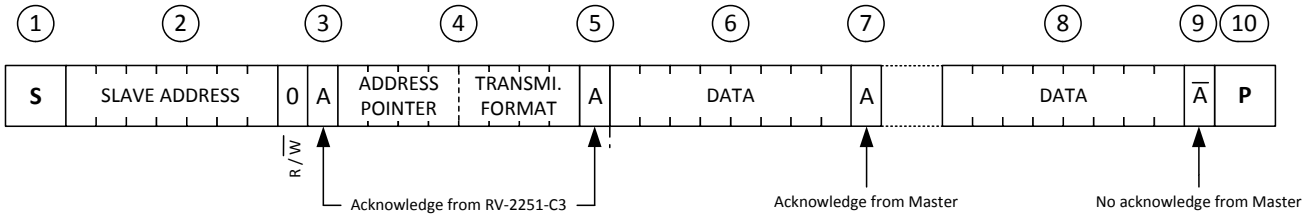


5.9.2.POWER SAVING READ AT SPECIFIC ADDRESS

This method of reading data from the internal register is started by reading immediately at specific address after writing to the 4-bit Address Pointer and the 4-bit Transmission Format field. Although this method is not based on I^2C-bus standard in a strict sense it is very effective to shorten read time and so to minimize MCU workload. Write 4h or 5h (010Xb) to the Transmission Format when this method is used.

Master reads data from slave RV-2251-C3 at specific address in power saving method:

1) Master sends out the START condition.
2) Master sends out Slave Address, 64h for the RV-2251-C3; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-2251-C3.
4) Master sends out the 4-bit Address Pointer and the 4-bit Transmission Format to RV-2251-C3.
   For the power saving write operation the Transmission Format must always be 0100b or 0101b.
5) Acknowledgement from RV-2251-C3.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
6) The Slave sends out the Data from the Address specified in step 4).
7) Acknowledgement from Master.
8) Steps 6) and 7) can be repeated if necessary.
   The Address Pointer is automatically incremented in the RV-2251-C3.
9) The Master, addressed as Receiver, can stop data transmission by not generating acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
10) Master sends out the STOP condition.

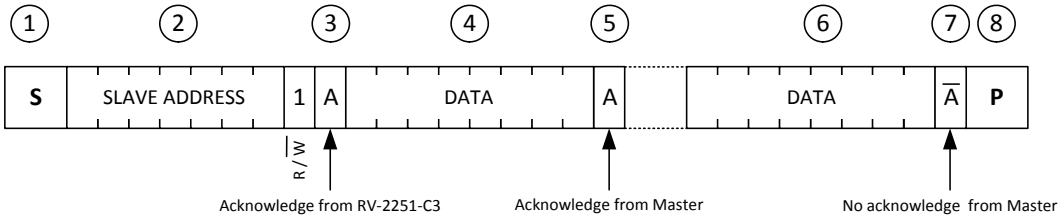


5.9.3.READ IMMEDIATELY

This method of reading data from the internal register is to start reading immediately after writing the Slave Address and setting R/$\overline{W}$ bit to 1. Since the Address Pointer is set to Fh by default because of a previous STOP condition, this method is only effective when reading is started from Address Fh.

Master reads data from slave RV-2251-C3 immediately after first byte:

1) Master sends out the START condition.
2) Master sends out Slave Address, 65h for the RV-2251-C3; the R/$\overline{W}$ bit is a 1 indicating a read operation.
3) Acknowledgement from RV-2251-C3.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
4) The RV-2251-C3 sends out the Data from the last accessed Register Address incremented by 1.
5) Acknowledgement from Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address is automatically incremented in the RV-2251-C3.
7) The Master, addressed as Receiver, can stop data transmission by not generating acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
8) Master sends out the STOP condition.



6. ELECTRICAL SPECIFICATIONS

6.1. ABSOLUTE MAXIMUM RATINGS

The following Table lists the absolute maximum ratings.

Absolute Maximum Ratings according to IEC 60134:

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{IO}	Peripheral Supply (I^2C, CLKOUT)		-0.3	6.5	V
V_{BAT}	Backup Power Supply		-0.3	6.5	V
V_{DD}	Main RTC Power Supply		-0.3	6.5	V
I_{DD}	Power supply current		-50	50	mA
V_I	Input voltage	Pins SCL, SDA and $\overline{ECO}$	-0.3	6.5	V
V_O	Output voltage 1	Pins SDA, $\overline{INT}$ and $\overline{V_{IOL}}$	-0.3	6.5	V
	Output voltage 2	Pin CLKOUT	-0.3	V_{IO} +0.3	V
	Output voltage 3	Pins V_{OUT} and V_{REG}	-0.3	V_{DD} +0.3	V
I_O	Output current	V_{OUT} and V_{REG}		10	mA
I_I	Input current	At any input	-10	10	mA
P_{TOT}	Total power dissipation	T_{OPR} = 25°C		300	mW
V_{ESD}	Electrostatic discharge Voltage	HBM (1)		±1500	V
		CDM (2)		±1000	V
I_{LU}	Latch-up current	(3)		100	mA
T_{OPR}	Operating temperature		-40	85	°C
T_{STO}	Storage temperature	Stored as bare product	-55	125	°C
T_{PEAK}	Maximum reflow condition	JEDEC J-STD-020C		265	°C

(1) HBM: Human Body Model, according to JESD22-A114.
(2) CDM: Charged-Device Model, according to JESD22-C101.
(3) Latch-up testing, according to JESD78, at maximum ambient temperature ($T_{A(max)}$)

6.2. OPERATING PARAMETERS

For this Table, V_{SS} = 0 V; V_{IO} = 3.0 V; V_{DD} = 3.3 V; V_{BAT} = 3.0 V; T_A = -40 °C to +85 °C; f_{OSC}= 32.768 kHz; TYP values at 25 °C; unless otherwise indicated.

Operating Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
$V_{DD:SUP}$	V_{DD} Power Supply	RTC supplied by V_{DD}	V_{DET1F}		5.5	V
$V_{IO:ACC}$	V_{IO} Peripheral Supply	Interface accessible	V_{DET2F}		5.5	V
$V_{OUT:TK}$	Timekeeping voltage		0.9		5.5	V
$V_{OUT:TKM}$	Minimum timekeeping voltage			0.7	0.9	V
V_{OF}	Oscillation failure voltage	$V_{OUT} \leq V_{OF}$, OF flag is set to 1		0.7	0.9	V
V_{PUP}	Pull-up voltage	Pins $\overline{INT}$ and $\overline{V_{IOL}}$			5.5	V
V_{BLF}	Backup voltage threshold	Pin V_{BAT}; T_A = -30 to +70°C	1.20	1.35	1.50	V
V_{DET1R}	Voltage detector 1 threshold; rising edge	Pin V_{DD}; T_A = 25°C	2.69	2.78	2.87	V
V_{DET1F}	Voltage detector 1 threshold; falling edge		2.62	2.70	2.78	
V_{DET1H}	Voltage detector 1 threshold; hysteresis			80		mV
V_{DET2R}	Voltage detector 2 threshold; rising edge	Pin V_{IO}; T_A = 25°C V_{OUT} = 1.0 V to 5.5 V	1.67	1.77	1.86	V
V_{DET2F}	Voltage detector 2 threshold; falling edge		1.61	1.70	1.79	
V_{DET2H}	Voltage detector 2 threshold; hysteresis			65		mV
t_{DELAY}	Output Delay Time of Voltage detector 2	Pin V_{IOL}; V_{OUT} = 1.0 V to 5.5 V	100	105	110	ms
V_{REG}	Voltage regulator output	Pin V_{REG}; T_A = 25°C; V_{DD} = 3.3 V; I_O = 1.0 mA	2.92	3.00	3.08	V
$\frac{\Delta V_{DET1,2}}{\Delta T_A}$	Voltage detector threshold temperature coefficients	Pins V_{DD} and V_{IO}; T_A = -40 °C to +85 °C	±100			ppm/°C
$\frac{\Delta V_{REG}}{\Delta T_A}$	Regulated voltage temperature coefficient	Pin V_{REG}; T_A = -40 °C to +85 °C	±100			ppm/°C
$I_{BAT:TK1}$	V_{BAT} timekeeping current 1; ECO mode on ($\overline{ECO}$ = LOW), BLF = 1 (monitoring off)	V_{BAT} = 3.0 V; V_{DD} = V_{IO} = 0 V; T_A = -40 °C to +85 °C (1)		210	650	nA
		V_{BAT} = 3.0 V; V_{DD} = V_{IO} = 0 V; T_A = -30 °C to +70 °C (1)			500	
$I_{BAT:TK2}$	V_{BAT} timekeeping current 2; ECO mode off ($\overline{ECO}$ = HIGH) BLF = 1 (monitoring off)	V_{BAT} = 3.0 V; V_{DD} = V_{IO} = 0 V; T_A = -40 °C to +85 °C (1)		270	800	nA
		V_{BAT} = 3.0 V; V_{DD} = V_{IO} = 0 V; T_A = -30 °C to +70 °C (1)			650	
I_{DD}	V_{DD} stand-by current	V_{DD} = 3.3 V		1.3		µA
I_{IO}	V_{IO} stand-by current	V_{IO} = 3.0 V		2.7		µA
$I_{DD:I2C}$	V_{DD} supply current during I^2C burst read/write	V_{DD} = 3.3 V, V_{IO} = 3.0 V 400 kHz bus speed, 2.2k pull-up resistors on SCL/SDA (2)		14	25	µA
$I_{IO:I2C}$	V_{IO} supply current during I^2C burst read/write			3	10	

(1) SCL = SDA = 0 V; CLKOUT = OPEN

(2) 2.2k pull-up resistors on SCL/SDA, excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0 V or V_{DD}. Test conditions: Continuous burst read/write, 55h data pattern, 25 µs between each data byte, 20 pF load on each bus pin.

For this Table, V_{SS} = 0 V; V_{IO} = 3.0 V; V_{DD} = 3.3 V; V_{BAT} = 3.0 V; T_A = -40 °C to +85 °C; f_{OSC}= 32.768 kHz; TYP values at 25 °C; unless otherwise indicated.

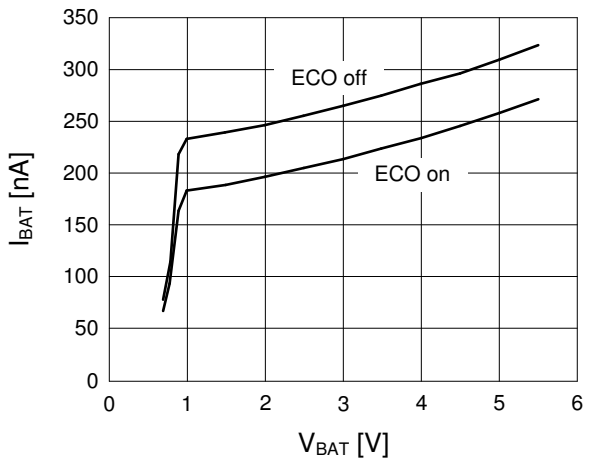
Operating Parameters (continued):

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Inputs						
$V_{IL:I2C}$	LOW level input voltage	Pins SCL and SDA; $V_{IO} = V_{DET2F}$ to 5.5 V	-0.3		0.2 V_{IO}	V
$V_{IH:I2C}$	HIGH level input voltage		0.8 V_{IO}		V_{IO}	V
$V_{IL:ECO}$	LOW level input voltage	Pin $\overline{ECO}$	-0.3		0.3	V
$V_{IH:ECO}$	HIGH level input voltage		V_{OUT} - 0.3		5.5	V
I_{LEAK}	Input leakage current	Pins SCL, SDA; V_{IO} = 5.5 V Pin $\overline{ECO}$; $V_I = V_{SS}$ or 5.5 V	-0.2		0.2	µA
C_I	Input capacitance	Pins SCL, SDA and $\overline{ECO}$			7	pF
Outputs						
$I_{OH:CLKOUT}$	HIGH level output current; Pin CLKOUT	$V_{OH:CLKOUT} = V_{IO}$ - 0.5 V	-0.5			mA
$I_{OL:CLKOUT}$	LOW level output current; Pin CLKOUT	V_{OL} = 0.4 V	0.5			mA
$I_{OL:INT}$	LOW level output current; Pin $\overline{INT}$		2.0			
$I_{OL:SDA}$	LOW level output current; Pin SDA		3.0			
$I_{OL:VIOL}$	LOW level output current; Pin $\overline{V_{IOL}}$	$V_{IO} = V_{DD} = V_{BAT}$ = 1.5 V (3) V_{OL} = 0.4 V	0.5			
I_{OZ}	Output Off-state current	Pin SDA; V_{IO} = 5.5 V Pins $\overline{INT}$ and $\overline{V_{IOL}}$; $V_O = V_{SS}$ or 5.5 V	-0.2		0.2	µA

(3) $V_{IO} < V_{DET2F}$

6.3. TYPICAL CHARACTERISTICS

Figure 1. Timekeeping current I_{BAT} vs. Supply voltage V_{BAT}: BLF not set back (no V_{BAT} sampling), T_A = 25°C



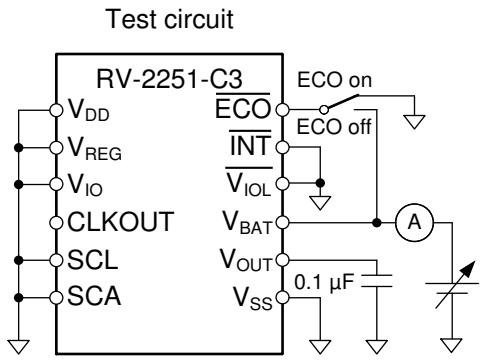
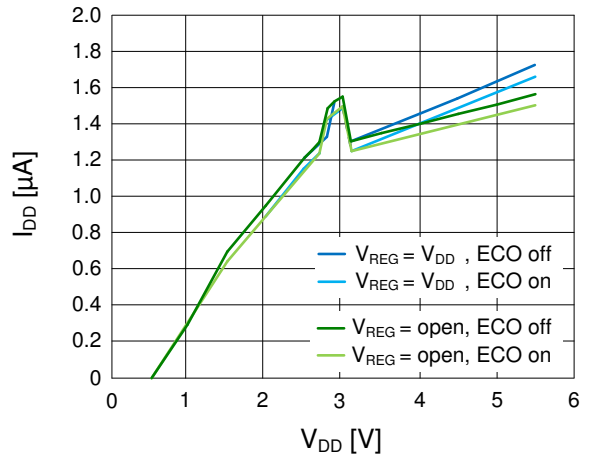


Figure 2. Stand-by current I_{DD} vs. Supply voltage V_{DD}: T_A = 25°C



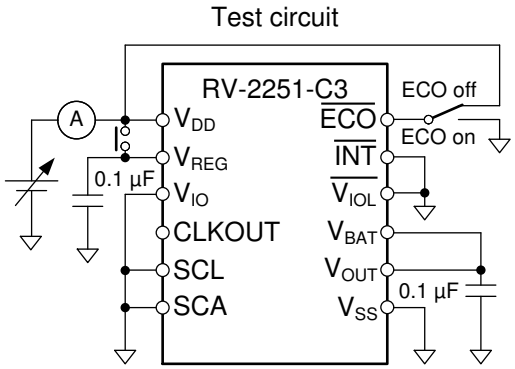
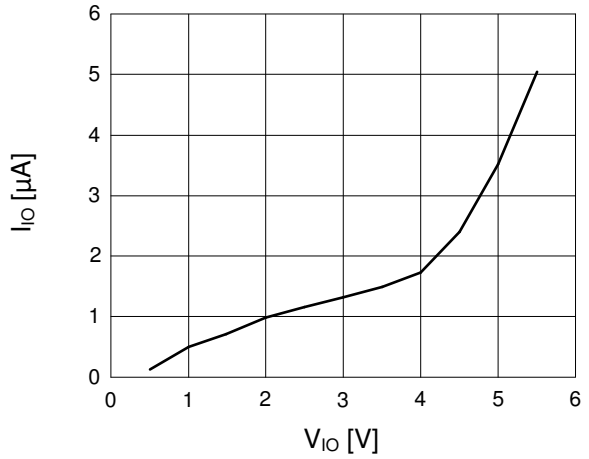


Figure 3. Stand-by current I_{IO} vs. Supply voltage V_{IO}: V_{DD} = 3.3 V (for V_{IO} monitoring and 32 kHz), T_A = 25°C



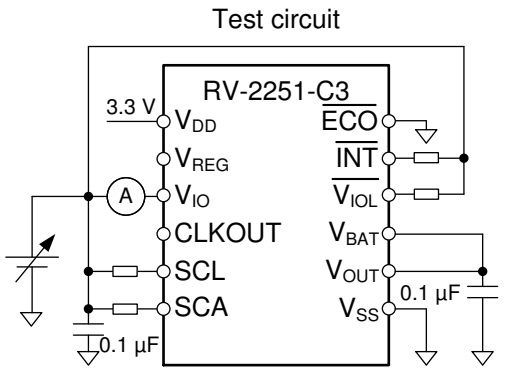
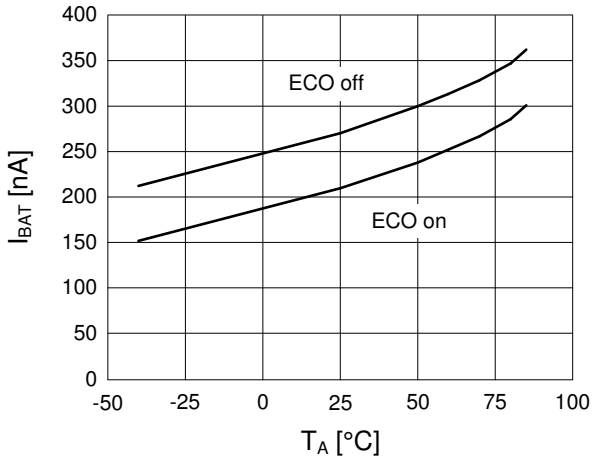


Figure 4. Timekeeping current I_{BAT} vs. Ambient temperature T_A: V_{BAT} = 3 V, V_{DD} = 0 V



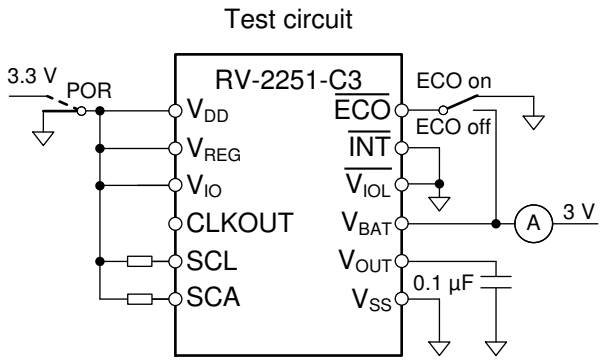
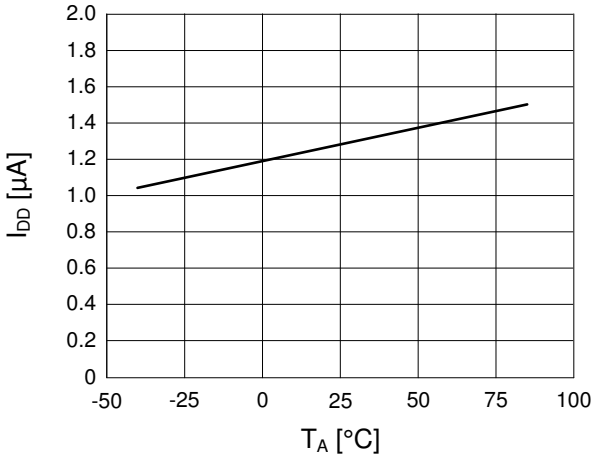


Figure 5. Stand-by current I_{DD} vs. Ambient temperature T_A: V_{DD} = 3.3 V, V_{BAT} = open



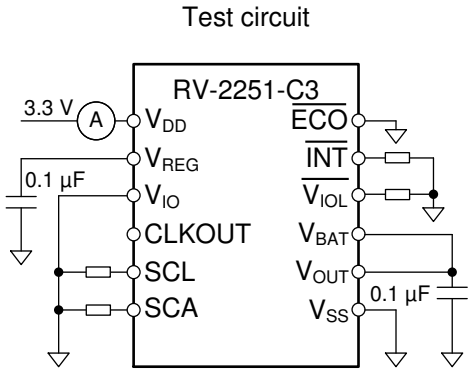
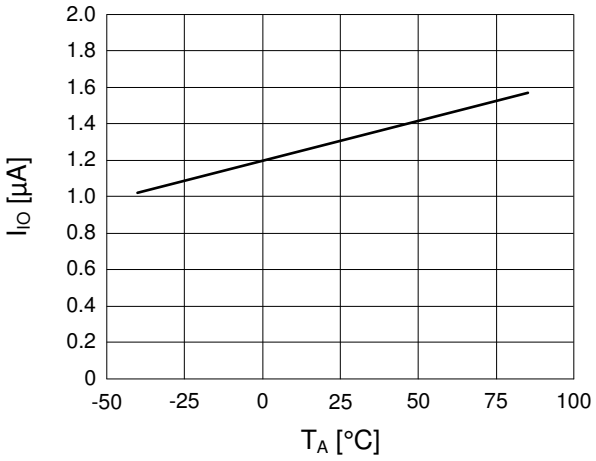


Figure 6. Stand-by current I_{IO} vs. Ambient temperature T_A: V_{IO} = 3.0 V, V_{DD} = 3.3 V (for V_{IO} monitor.), V_{BAT} = open



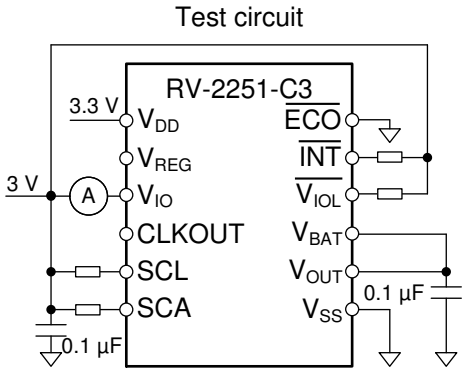
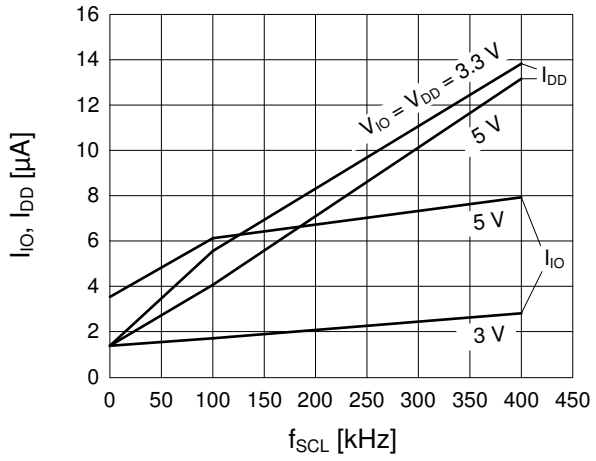


Figure 7. MCU access current I_{IO}/I_{DD} vs. SCL clock frequency f_{SCL}: See conditions in section 6.2, T_A = 25°C



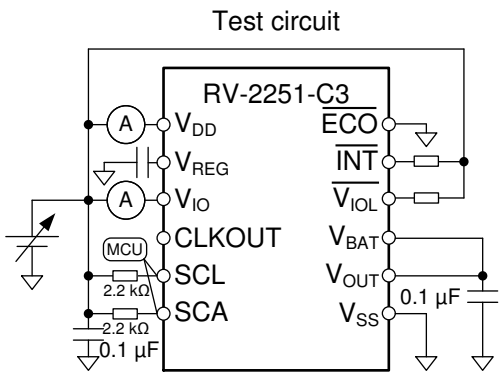
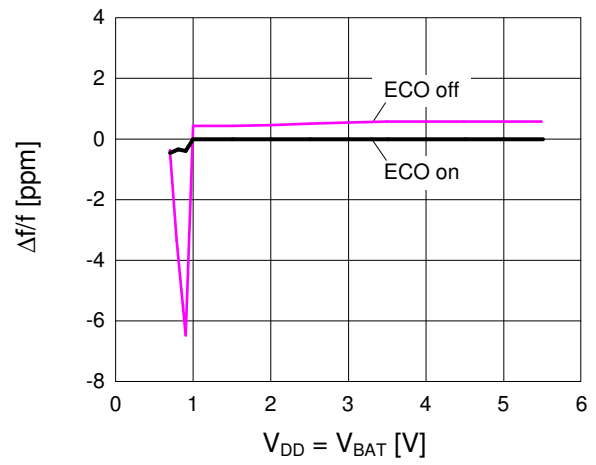


Figure 8. Frequency deviation Δf/f vs. Supply voltage $V_{DD} = V_{BAT}$ (normalized ECO on, 3 V): V_{IO} = 3 V, T_A = 25 °C



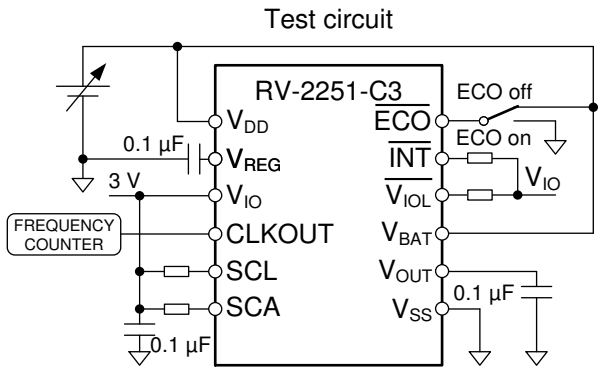
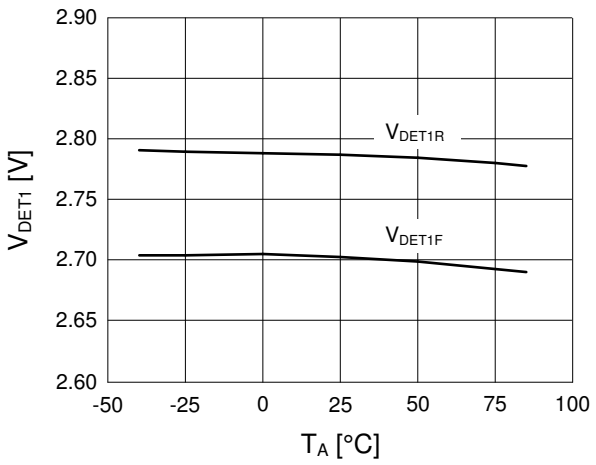


Figure 9. Detector threshold voltage (V_{DET1R}/V_{DET1F}) vs. Ambient temperature T_A (V_{DD} monitoring):



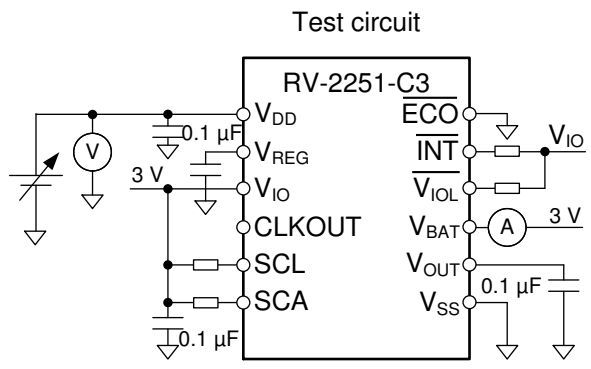
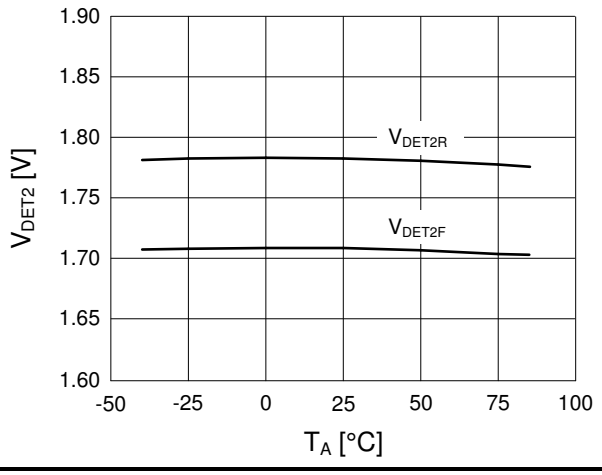


Figure 10. Detector threshold voltage (V_{DET2R}/V_{DET2F}) vs. Ambient temperature T_A (V_{IO} monitoring):



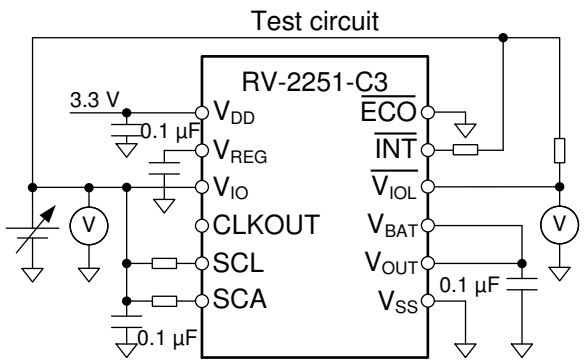
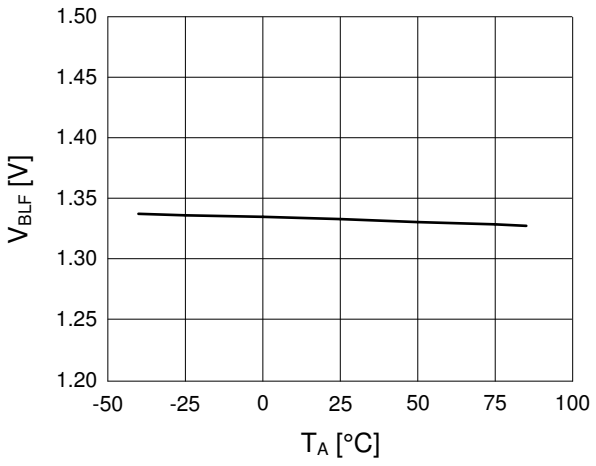


Figure 11. Detector threshold voltage V_{BLF} vs. Ambient temperature T_A (V_{BAT} monitoring):



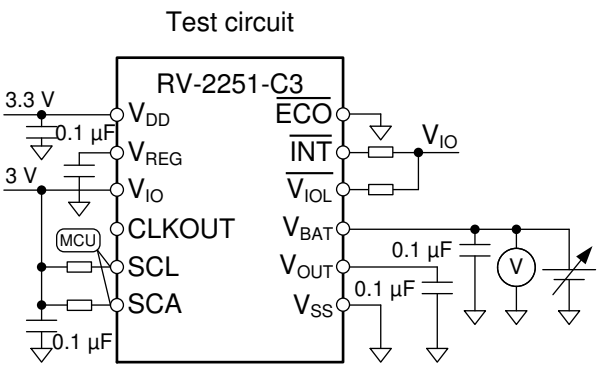
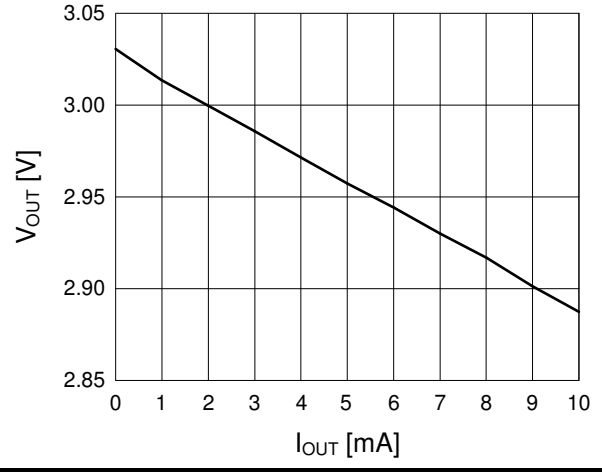


Figure 12. V_{OUT} vs. Output load current I_{OUT} (voltage after regulator and SW1): V_{DD} = 3.3 V, T_A = 25 °C



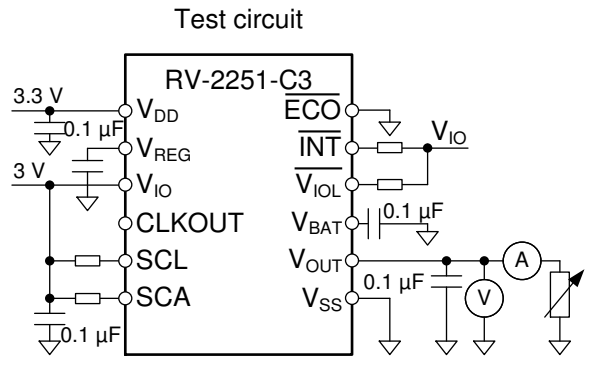


Figure 13. V_{OUT} - (V_{REG} = V_{DD}) vs. Output load current I_{OUT} (voltage drop SW1, V_{DD} > V_{DET1}): T_A = 25 °C

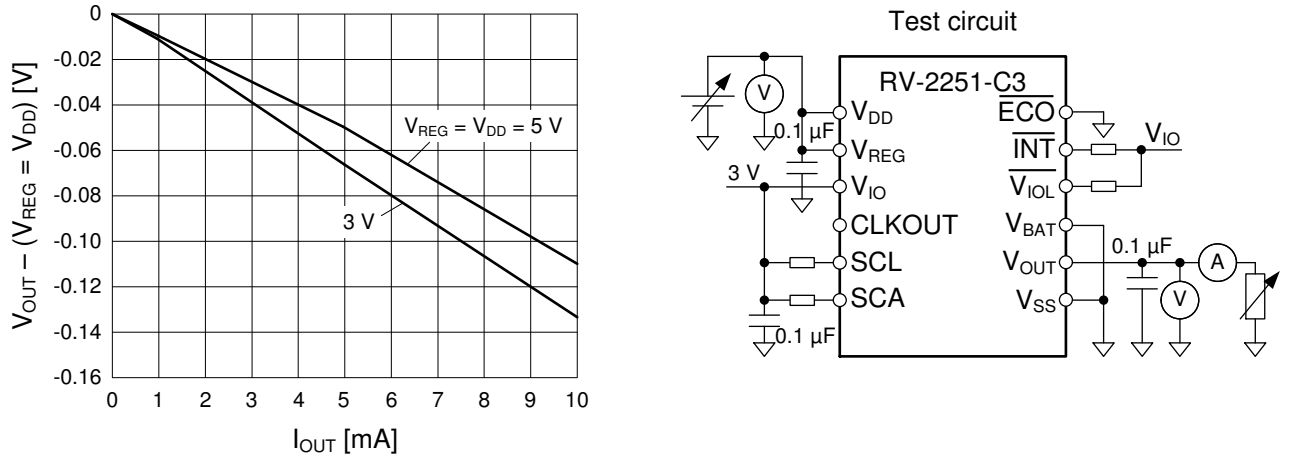


Figure 14. V_{OUT} - V_{BAT} vs. Output load current I_{OUT} (voltage drop SW2): T_A = 25 °C

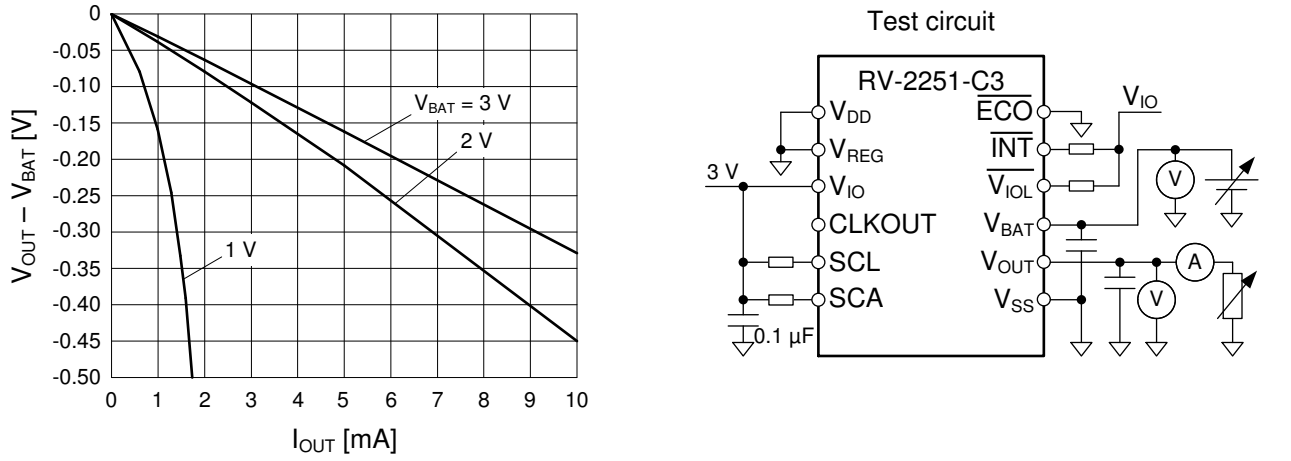


Figure 15. V_{OUT} vs. V_{DD}: Measured on falling edge of V_{DD} (V_{DET1F} = 2.70 V), V_{REG} floating, T_A = 25°C

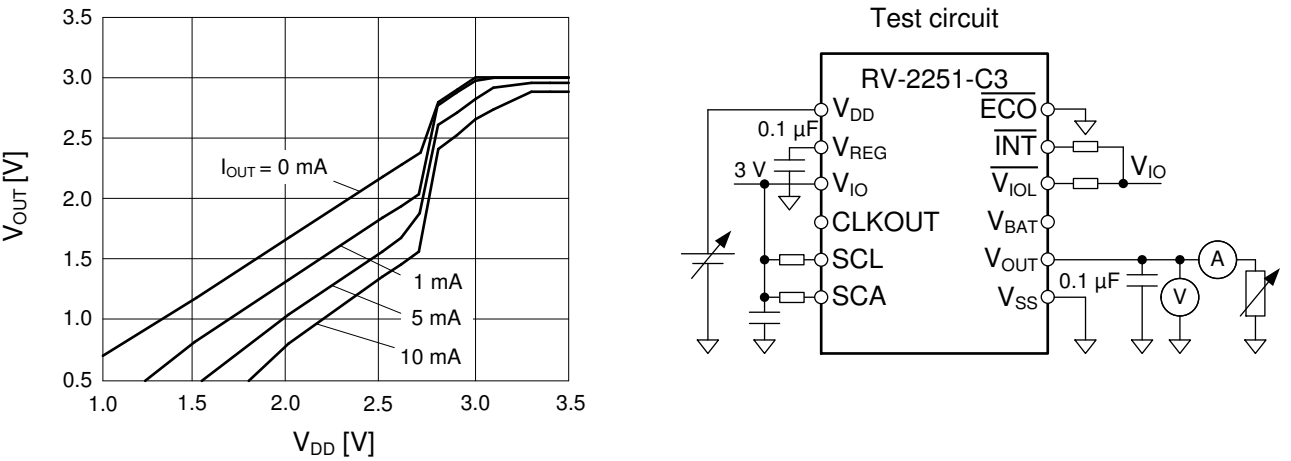
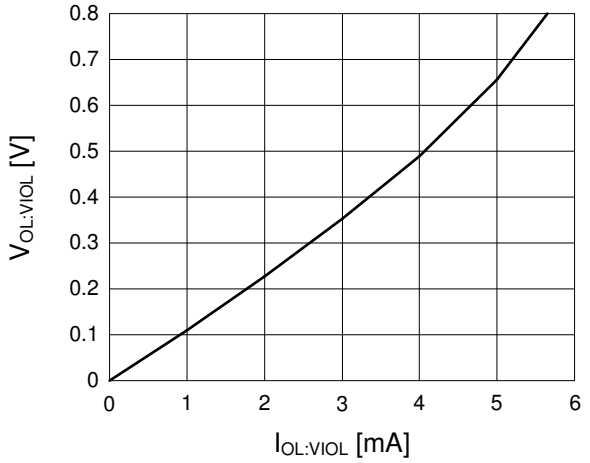


Figure 16. $V_{OL:VIOL}$ vs. $I_{OL:VIOL}$ ($\overline{V_{IOL}}$ pin) : $V_{IO} < V_{DET2F}$ (V_{DET2F} = 1.70 V), $V_{BAT} = V_{DD} = V_{IO}$ = 1.5 V, T_A = 25 °C



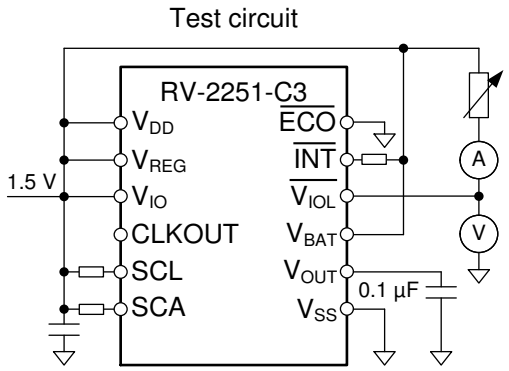
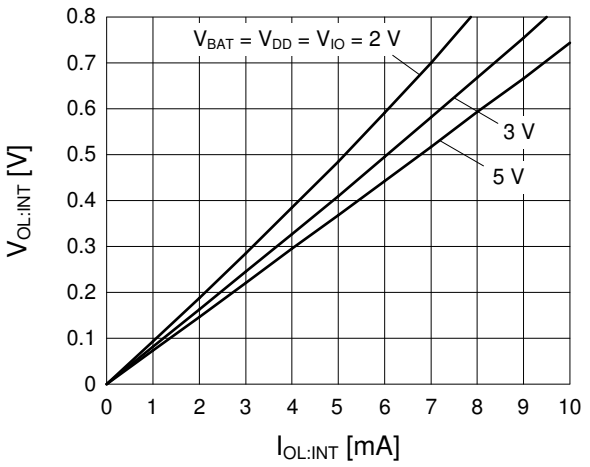
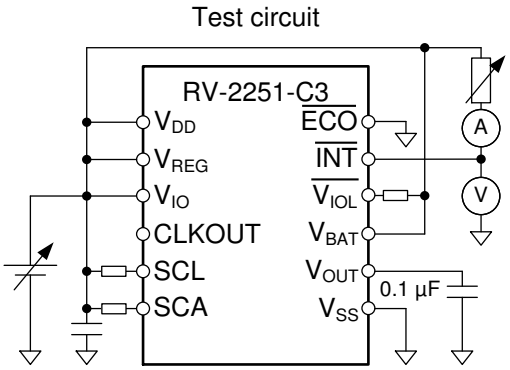


Figure 17. $V_{OL:INT}$ vs. $I_{OL:INT}$ ($\overline{INT}$ pin): $V_{BAT} = V_{DD} = V_{IO}$, T_A = 25 °C





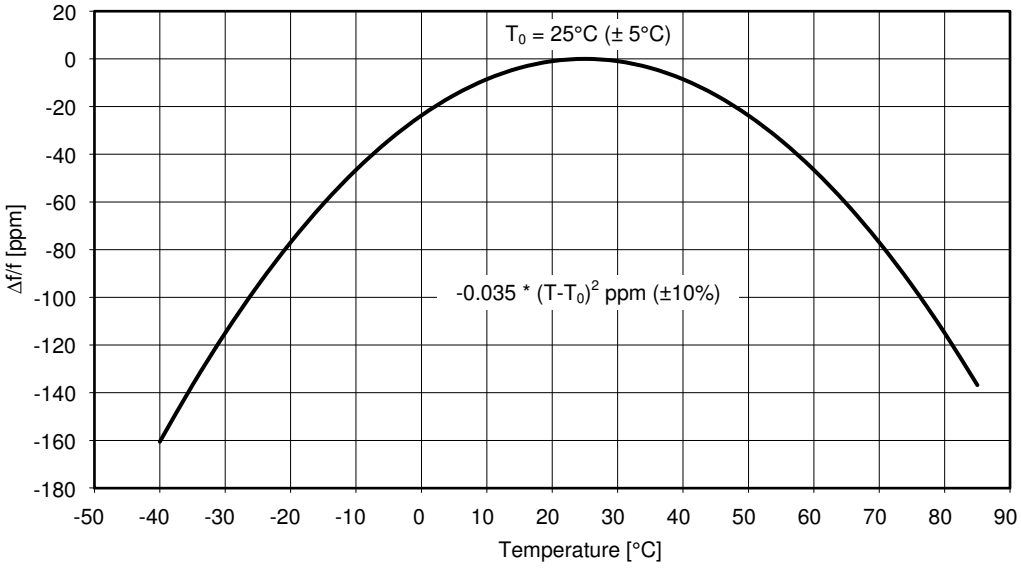
6.4. OSCILLATOR PARAMETERS

For this Table, V_{SS} = 0 V; V_{IO} = 3.0 V; V_{DD} = 3.3 V; V_{BAT} = 3.0 V; T_A = -40 °C to +85 °C; f_{OSC}= 32.768 kHz; TYP values at 25 °C; unless otherwise indicated.

Oscillator Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Xtal General						
f	Crystal Frequency			32.768		kHz
t_{START}	Oscillator start-up time	V_{OUT} = 3.0 V		100	500	ms
δ_{CLKOUT}	CLKOUT duty cycle	f_{CLKOUT} = 32.768 kHz T_A = 25°C	40		60	%
Xtal Frequency Characteristics						
Δf/f	Frequency accuracy	f = 32.768 kHz T_A = 25°C		±10	±20	ppm
$\Delta f/f_{TOPR}$	Frequency vs. temperature characteristics	T_{OPR} = -40°C to +85°C V_{DD} = 3.3 V	$-0.035^{ppm}/_{°C}{}^2 (T_{OPR}-T_0)^2$ ±10%			ppm
T_0	Turnover temperature		20		30	°C
Δf/f	Aging first year max.	T_A = 25°C, V_{DD} = 3.3 V			±3	ppm
Frequency Offset Compensation						
Δt/t	OFFSET value MODE = 0 Min. comp. step (LSB) and Max. comp. range	T_A = -40°C to +85°C	±3.052		±189	ppm
Δt/t	OFFSET value MODE = 1 Min. comp. step (LSB) and Max. comp. range	T_A = -40°C to +85°C	±1.017		±63	ppm
Δt/t	Achievable time accuracy MODE = 0	Calibrated at an initial temperature	-1.5		+1.5	ppm
			-0.13		+0.13	s/day
Δt/t	Achievable time accuracy MODE = 1	Calibrated at an initial temperature	-0.5		+0.5	ppm
			-0.04		+0.04	s/day

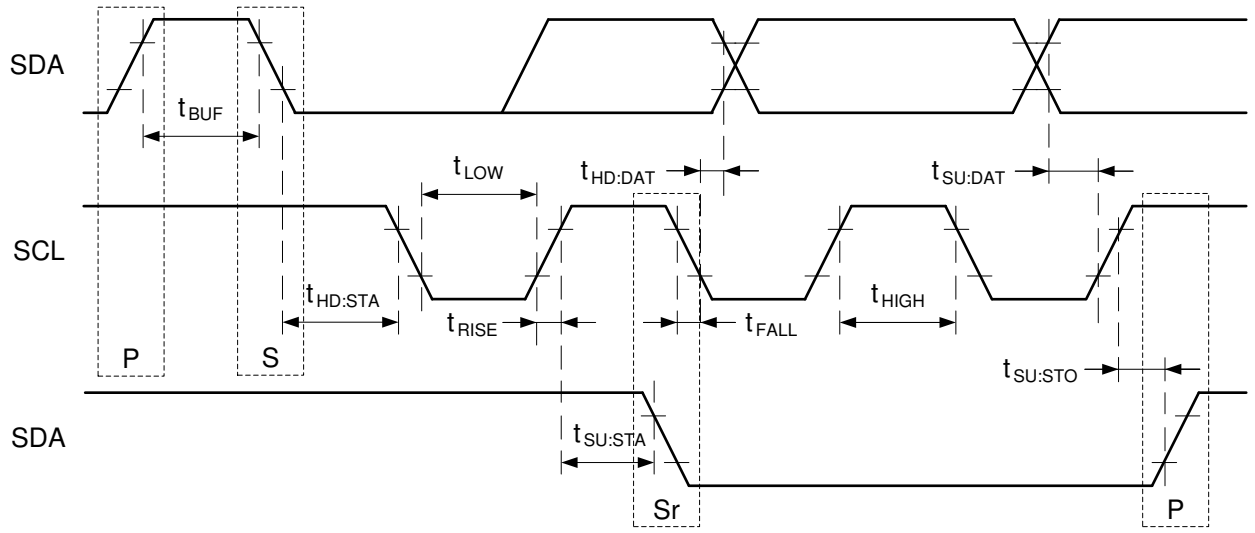
6.4.1.XTAL FREQUENCY VS. TEMPERATURE CHARACTERISTICS



6.5. I²C-BUS INTERFACE AC ELECTRICAL CHARACTERISTICS

The following Figure and Table describe the I²C-bus interface AC electrical parameters.

I²C-bus interface AC Parameter Definitions:



For the following Table, T_A = -40 °C to 85 °C, TYP values at 25 °C.

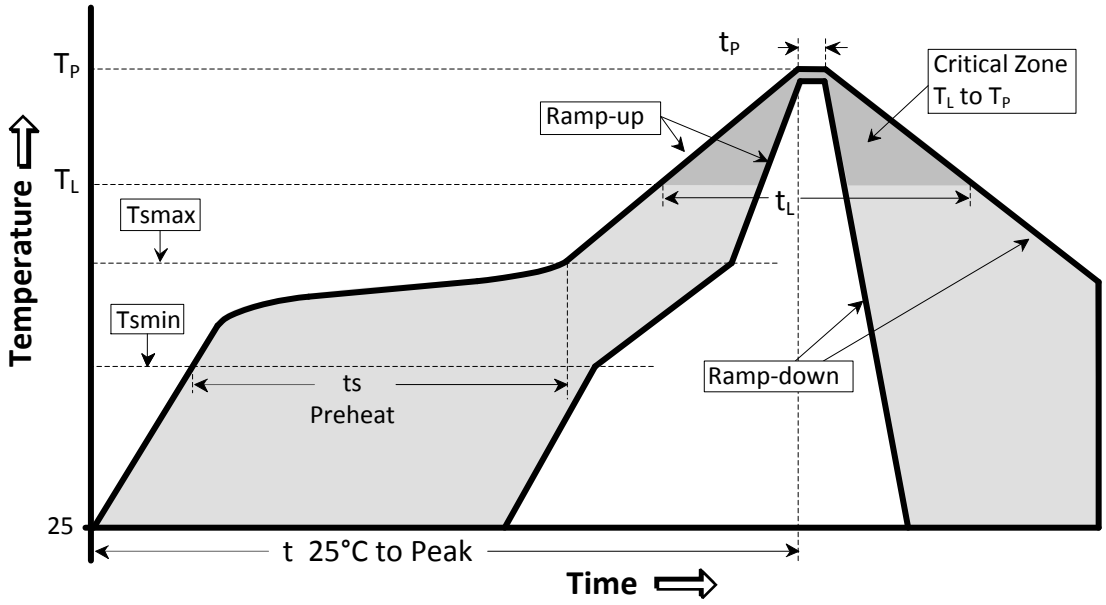
I²C-bus interface AC Electrical Parameters:

SYMBOL	PARAMETER	Conditions	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	$V_{IO} = V_{IO:ACC}$			400	kHz
t_{LOW}	Low period of SCL clock	$V_{IO} = V_{IO:ACC}$	1.3			µs
t_{HIGH}	High period of SCL clock	$V_{IO} = V_{IO:ACC}$	0.6			µs
t_{RISE}	Rise time of SDA and SCL	$V_{IO} = V_{IO:ACC}$			300	ns
t_{FALL}	Fall time of SDA and SCL	$V_{IO} = V_{IO:ACC}$			300	ns
$t_{HD:STA}$	START condition hold time	$V_{IO} = V_{IO:ACC}$	0.6			µs
$t_{SU:STA}$	START condition setup time	$V_{IO} = V_{IO:ACC}$	0.6			µs
$t_{SU:DAT}$	SDA setup time	$V_{IO} = V_{IO:ACC}$	100			ns
$t_{HD:DAT}$	SDA hold time	$V_{IO} = V_{IO:ACC}$	0			µs
$t_{SU:STO}$	STOP condition setup time	$V_{IO} = V_{IO:ACC}$	0.6			µs
t_{BUF}	Bus free time before a new transmission	$V_{IO} = V_{IO:ACC}$	1.3			µs
S = Start condition, Sr = Repeated Start condition, P = Stop condition						

Caution:
When communicating with the RV-2251-C3 module, the series of operations from transmitting the START (or repeated START) condition to transmitting the STOP (or repeated START) condition should occur within 0.5 second. If this series of operations requires 0.5 second or more, the I²C bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-2251-C3 module.

7. RECOMMENDED REFLOW TEMPERATURE (LEAD-FREE SOLDERING)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



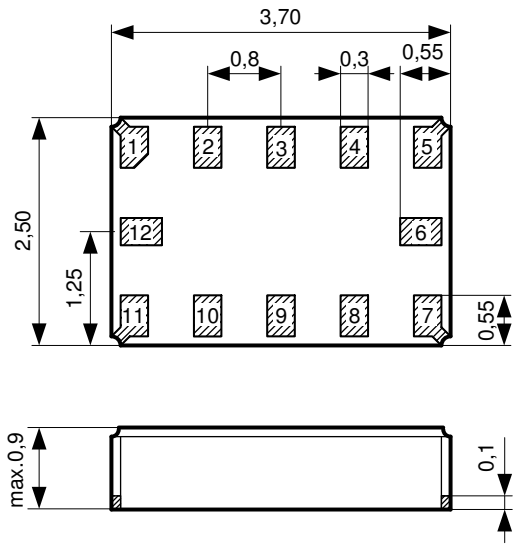
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to T_P)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	min
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 – 40	sec

8. PACKAGE

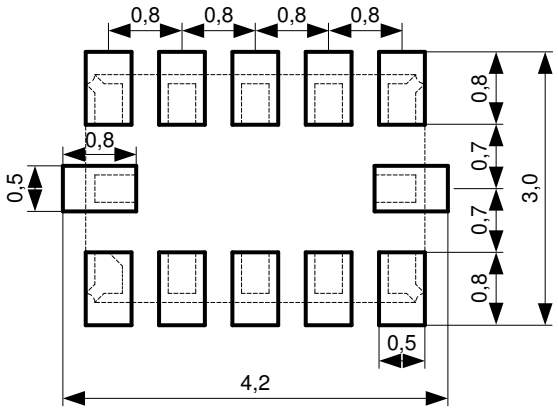
8.1. DIMENSIONS AND SOLDER PAD LAYOUT

C3 Package:

Package dimensions (bottom view):



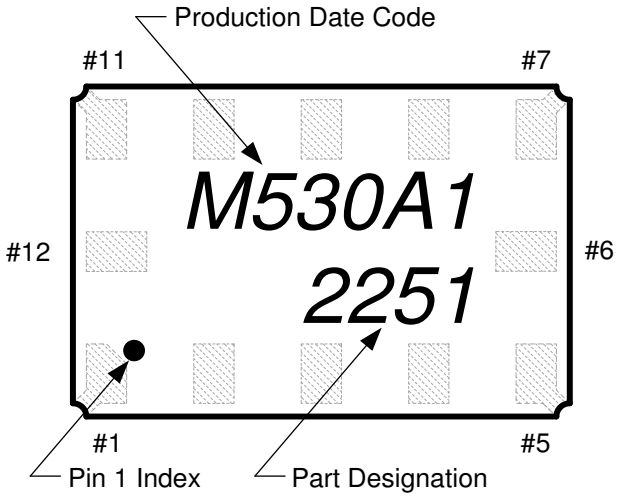
Recommended solder pad layout:



All dimensions in mm typical.

8.2. MARKING AND PIN #1 INDEX

C3 Package: (top view)

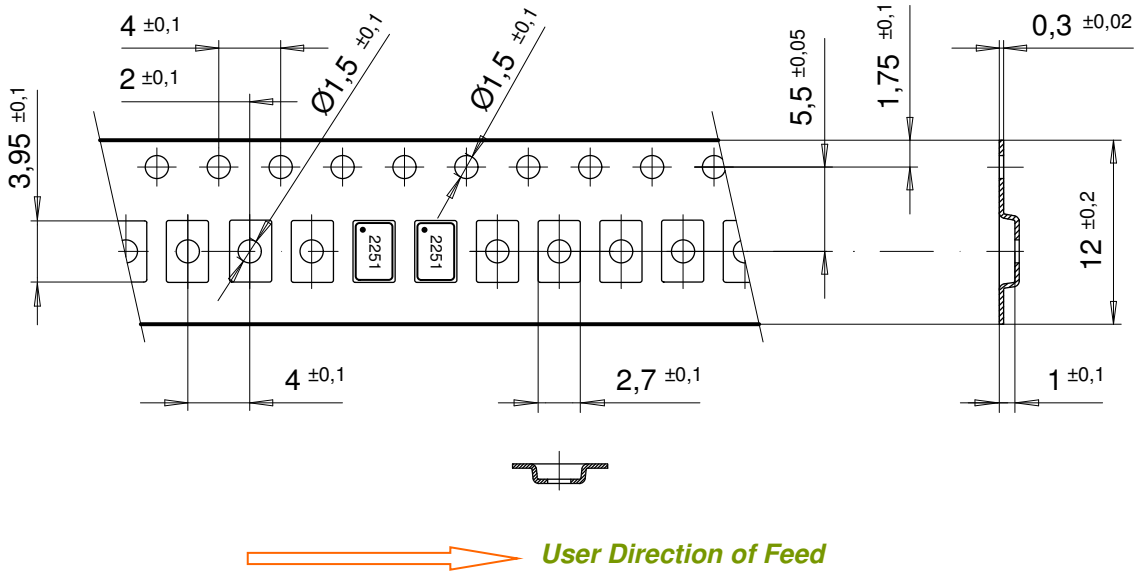


9. PACKING INFORMATION

9.1. CARRIER TAPE

12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer
	Peel Method:	Middle part removed, sticky sides remain on carrier

C3 Package:



Tape Leader and Trailer: 300 mm minimum.
All dimensions in mm.

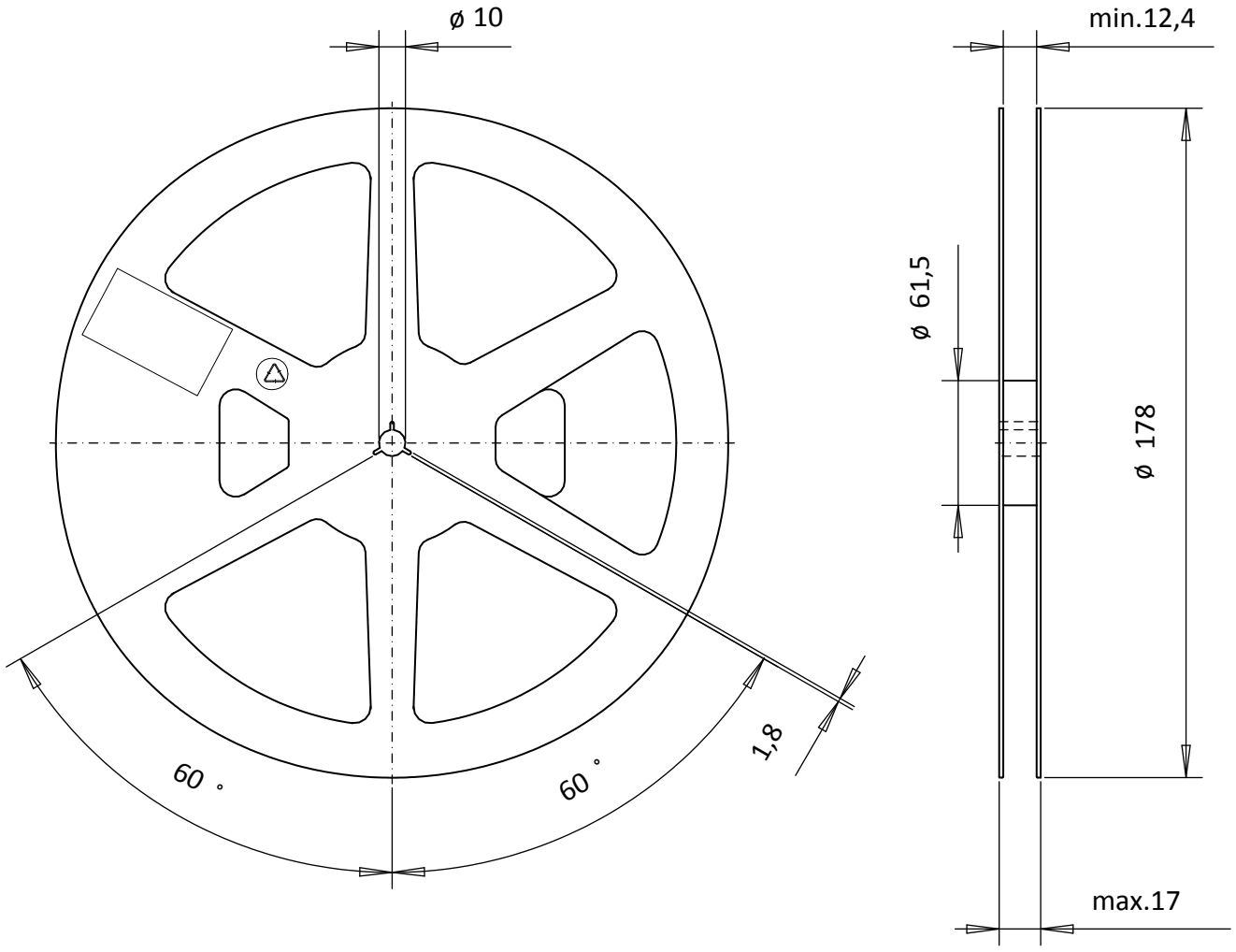
9.2. PARTS PER REEL

C3 Package:

Reels:

Diameter	Material	RTC's per reel
7"	Plastic, Polystyrol	1'000
7"	Plastic, Polystyrol	3'000

9.3. REEL 7 INCH FOR 12 mm TAPE



Reel:

Diameter	Material
7”	Plastic, Polystyrol

9.4. HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal / module will bear a mechanical shock of 5000g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage crystals due to mechanical resonance of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for rework:

- Use a hot-air- gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

10. DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
January 2016	1.0	First release