ERRATA SHEET
RV-8803-C7

Silicon Limitation

A COMPANY OF THE SWATCH GROUP

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1. DEVICE LIMITATION I²C COMMUNICATION

1.1. SILICON IDENTIFICATION

Production date code: M xxx yy
xxx = 412 and higher
yy = various
Part Designation: 8803

1.2. DESCRIPTION

The RV-8803-C7 has a built-in Watchdog function to autonomously RESET the I²C Interface after a Bus-Timeout of 950 ms.
There is a short time window where the RESET is triggered erroneously. With standard I²C-bus firmware, checking the Acknowledge, there are no false results.
Due to the automatic initialization of the I²C timeout function at I²C START it is possible that the RV-8803-C7 triggers an erroneous Bus-Timeout Reset and consequently responds with “no acknowledge” for the duration of maximum 61 µs. This unwanted Bus-Timeout Reset of the I²C Interface occurs when a START condition is sent 950 ms + n * 1000 ms (n = 0, 1, 2, …) after a previous START condition.

1.3. PROBABILITY

The RV-8803-C7 will only send the “no acknowledge” for 10 ms if the consecutive communication is taking place 950 ms after the previous one.
The probability to hit the critical time window is slim: 10 ms / 1.0 s, equal to the ratio of 1:100.

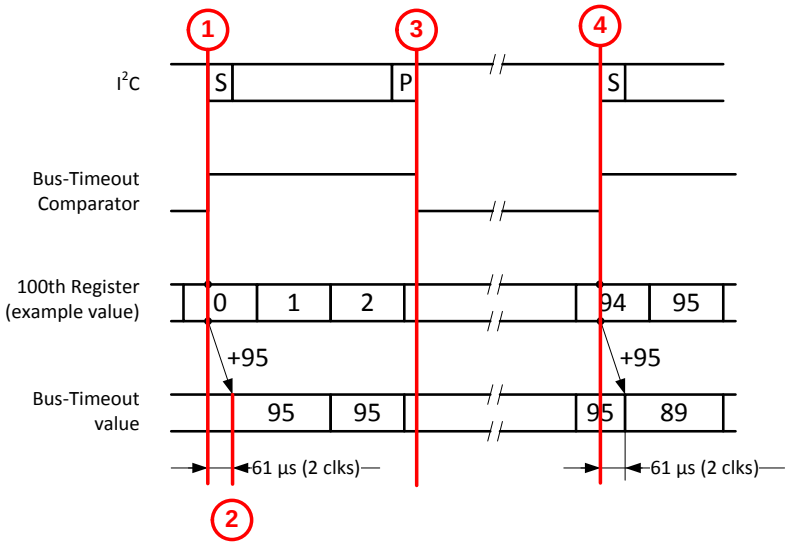
1.4. WORKAROUND

Software has to verify every acknowledgement from RV-8803-C7 and when a “no acknowledge” is detected has to begin communication procedure again with the I²C Start condition.

1.5. DETAILED DESCRIPTION

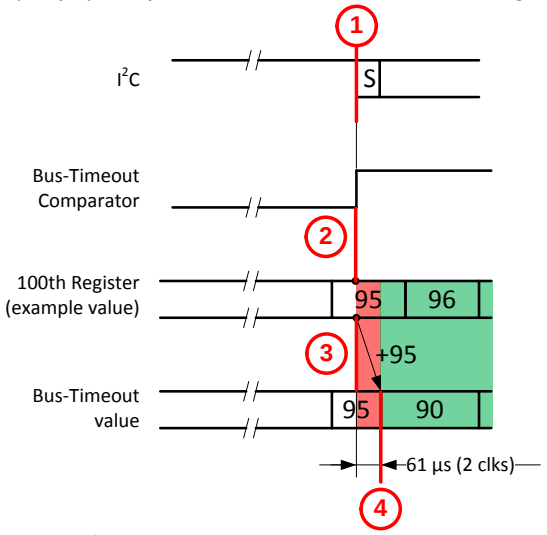
Initialization of the I²C Interface Bus-Timeout by RV-8803-C7:

1. At START condition, the Bus-Timeout Comparator is enabled.
2. It takes 2 clocks 32'768 Hz (61 µs) to read the value of the 1/100th seconds, adding 95/100th and write this as a Bus-Timeout target into the comparator.
3. At STOP condition, the comparator is disabled.
4. At the consecutive START (after STOP), the comparator is enabled with previous Bus-Timeout target value before the next value is calculated and written into the comparator.



Erroneous Bus-Timeout Reset Scenario 1: New START exactly 950 ms after previous START.

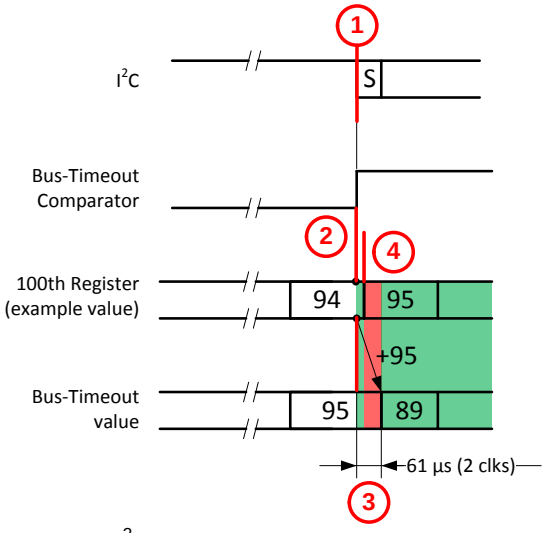
1. At START condition, the comparator is enabled.
2. At the consecutive START the comparator is enabled with previous Bus-Timeout target value.
3. If the actual 1/100th of Second matches with the previous Bus-Timeout target value, a RESET of the I^2C Interface will be triggered immediately.
4. It takes 2 clocks 32'768 Hz (61 µs) to update the new Bus-Timeout target value.



Summarized: At START condition of the I^2C Interface the Bus-Timeout comparator is enabled. If there is a match between the current value in the 1/100th Seconds register and the previous Bus-Timeout value, the comparator triggers an I^2C Bus-Timeout RESET and the RV-8803-C7 will reply immediately with "no acknowledge".

Erroneous Bus-Timeout Reset Scenario 2: New START shortly before 950 ms after previous START

1. At START condition, the comparator is enabled.
2. At the consecutive START the comparator is enabled with previous Bus-Timeout target value. As long as no match with the current 1/100th second is detected no RESET will be triggered.
3. It takes 2 clocks 32'768 Hz (61 µs) to update the new Bus-Timeout target value.
4. If during the 61 µs required for up-dating the Bus-Timeout value the 1/100th of Second is incremented and match the previous Bus-Timeout target value, the I^2C Interface will be RESET.



Summarized: At START condition of the I^2C Interface the Bus-Timeout comparator is enabled. The 1/100th Seconds register might have the value "previous Bus-Timeout value less one" and the RV-8803-C7 will replay with acknowledge. As soon as the there is a match between the current value in the 1/100th Seconds register and the previous set Bus-Timeout value, the comparator triggers an I^2C Bus-Timeout RESET and the RV-8803-C7 will reply with "no acknowledge".

1.6. WORKAROUND DETAILED

It's recommended to follow I^2C standard protocol and check ACK "acknowledge". When "no acknowledge" is detected, repeat communication procedure beginning with I^2C Start.

Based on the worst-case combination, a maximum of three consecutive i2c_write(); accesses may fail due to a Bus-Timeout RESET and respond with "no acknowledge":

- most unlucky timing interval of the START condition
- maximum I^2C Interface clock-speed (400 kHz)
- maximum 61 µs requirement up-dating the Bus-Timeout.

Workaround: Repeat I^2C communication procedure maximum 4 x times.

2. DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
April 2016	1.0	First release
May 2016	1.1	Completed description, 1.2. Added probability, 1.3.